Data Sheet, V 1.3, Oct. 2003

TC1920

32-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

Edition 2003-10

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Data Sheet, V 1.3, Oct. 2003

TC1920

32-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

TC1920
Preliminary
Revision History: 2003-10 V 1.3

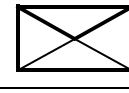
Previous Version: 1.2

Page	**Subjects (major changes since last revision)**
	ASC and SSC baudrates calculated for 50 MHz
	DC parameters updated with characterization values
	AC parameters updated with characterization values

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com



Preliminary

TC1920 Features

The TC1920 offers a 32 bit TriCore based microcontroller/DSP, which is mainly designed for automotive telematics applications. Due to its high integration, this microcontroller/DSP offers high system performance at minimized cost. Typical telematics functions processed by RISC-, DSP- and speech- (CODEC) modules are now combined in one component. The combination of dedicated automotive peripherals (CAN, J1850) and standard peripherals (ADC, SSC/SPI, ASC and IIC), makes this microcontroller/DSP the engine tailored for a wide variety of telematics applications such as navigation, emergency call, speech interface or communication interface.

- TriCore CPU/DSP with 4-Stage Pipeline:
  - 100 MHz max. CPU clock frequency, 50 MHz max. FPI Bus clock frequency.
  - 32-bit super-scalar TriCore main CPU
  - 4-GByte unified memory space support
  - Fast context-switching
  - Dual 16 x 16 Multiply-Accumulate (MAC) Unit
  - 64-bit Local Memory Bus (LMB)
  - 32-bit Flexible Peripheral Interface (FPI)
  - 32-bit wide external bus unit (EBU)
- 32-bit Peripheral Control Processor (PCP2) with DMA-support
- On-chip memories:
  - 24 KByte Code Scratch-Pad RAM (CSRAM)
  - 8 KByte Instruction Cache (ICACHE)
  - 24 KByte Data Scratch-Pad RAM (DSRAM)
  - 8 KByte Data Cache (DCACHE)
  - 64 KByte fast LMB SRAM
  - 16 KByte FPI SRAM (of which 8 KByte Stand-By SRAM)
  - 20 KByte PCP RAM: 16 KByte Code and 4 KByte Data SRAM
  - 32 KByte Boot ROM
- Product Specific Peripherals:
  - 14-bit double CODEC with flexible sample rates and FIFO support
- Automotive Peripherals:
  - Two independent CAN-nodes (TwinCAN) with gateway support
  - J1850 (SDLM)
- Standard Peripherals:
  - 6-channel, 8-/10-/12-bit ADC
  - 3 x asynchronous serial interface (ASC) with IrDa-support
  - 1 SPI-compatible synchronous serial interface
  - 2-channel IIC
  - 6 x 32 bit timer
  - ≥ 16 I/O- and interrupt pins (GPIO)
- General Peripherals:
  - Real time clock (RTC)

Preliminary

  - Watchdog timer (WDT)
- Clock Generation Unit with PLL
- Debug Support:
  - Debug Interface (OCDS level 2) with Trace Port
- Power saving features
- Dual voltage supply (1.8V core, 3.3V I/O)
- -40°C to +85°C temperature range
- LBGA-260 package

Preliminary

Block Diagram

The figure below shows the block diagram of the TC1920 device.

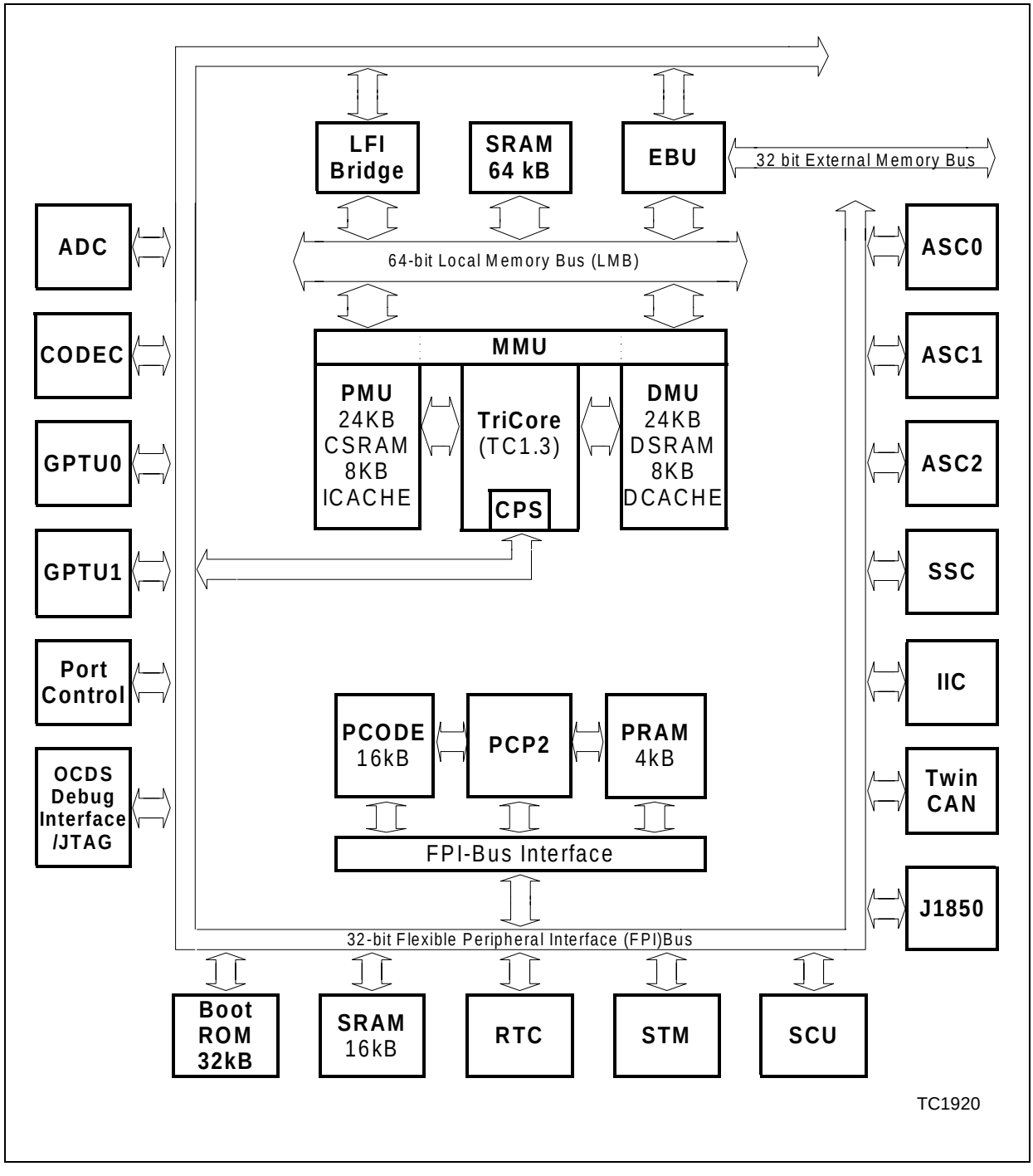


Figure 1 TC1920 Device Block Diagram

Preliminary

Target applications

- On-board and off-board navigation
- Emergency call systems
- Car speech interface
- Car communication interface
- Gateways: automotive - infotainment
- Occupant Sensing
- Drowsiness detection
- Rear- & side-mirror replacement
- Pre-crash sensing

Logical Symbol

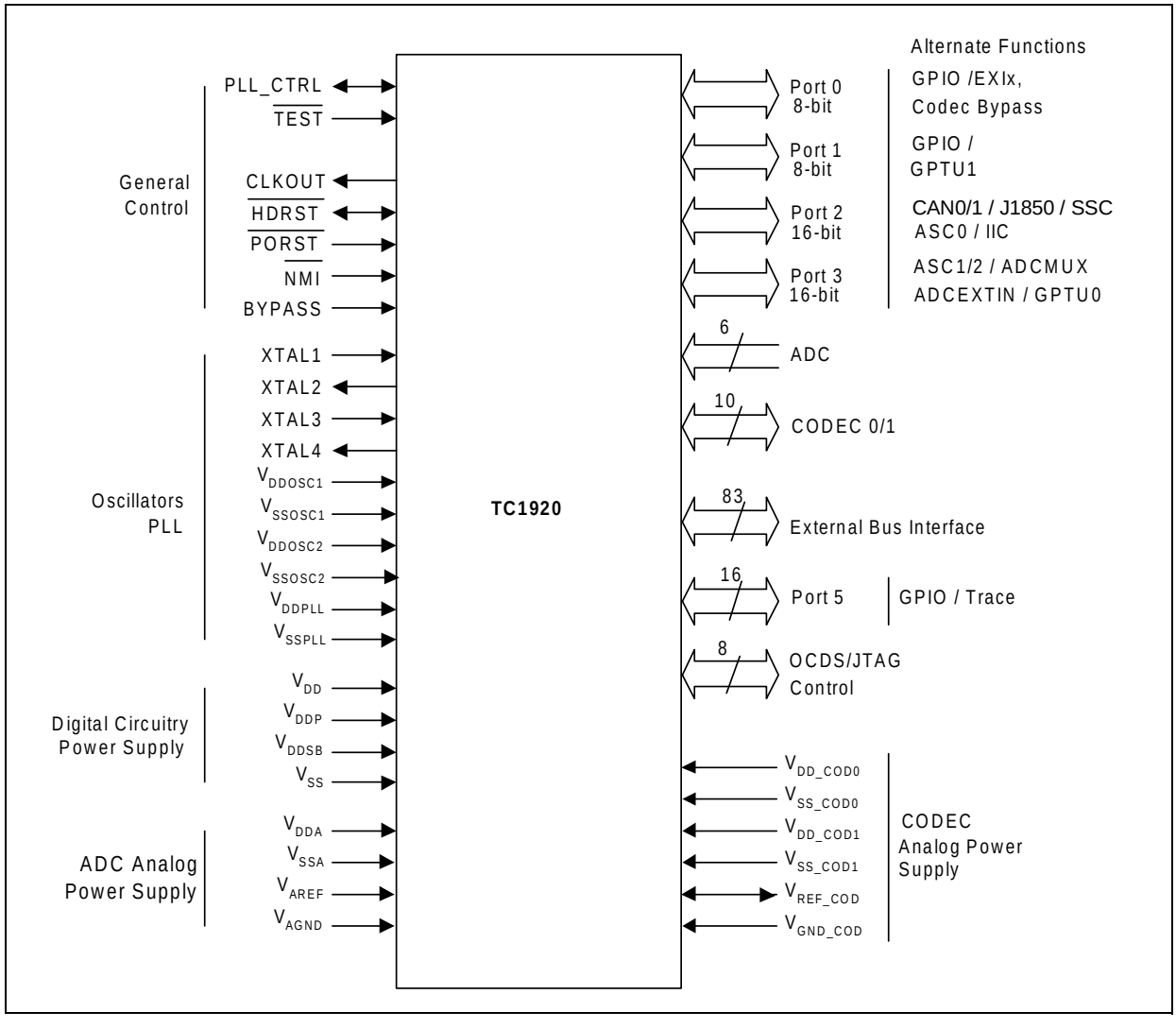


Figure 2 Logical Symbol of the TC1920 Device

Preliminary

Pin Configuration

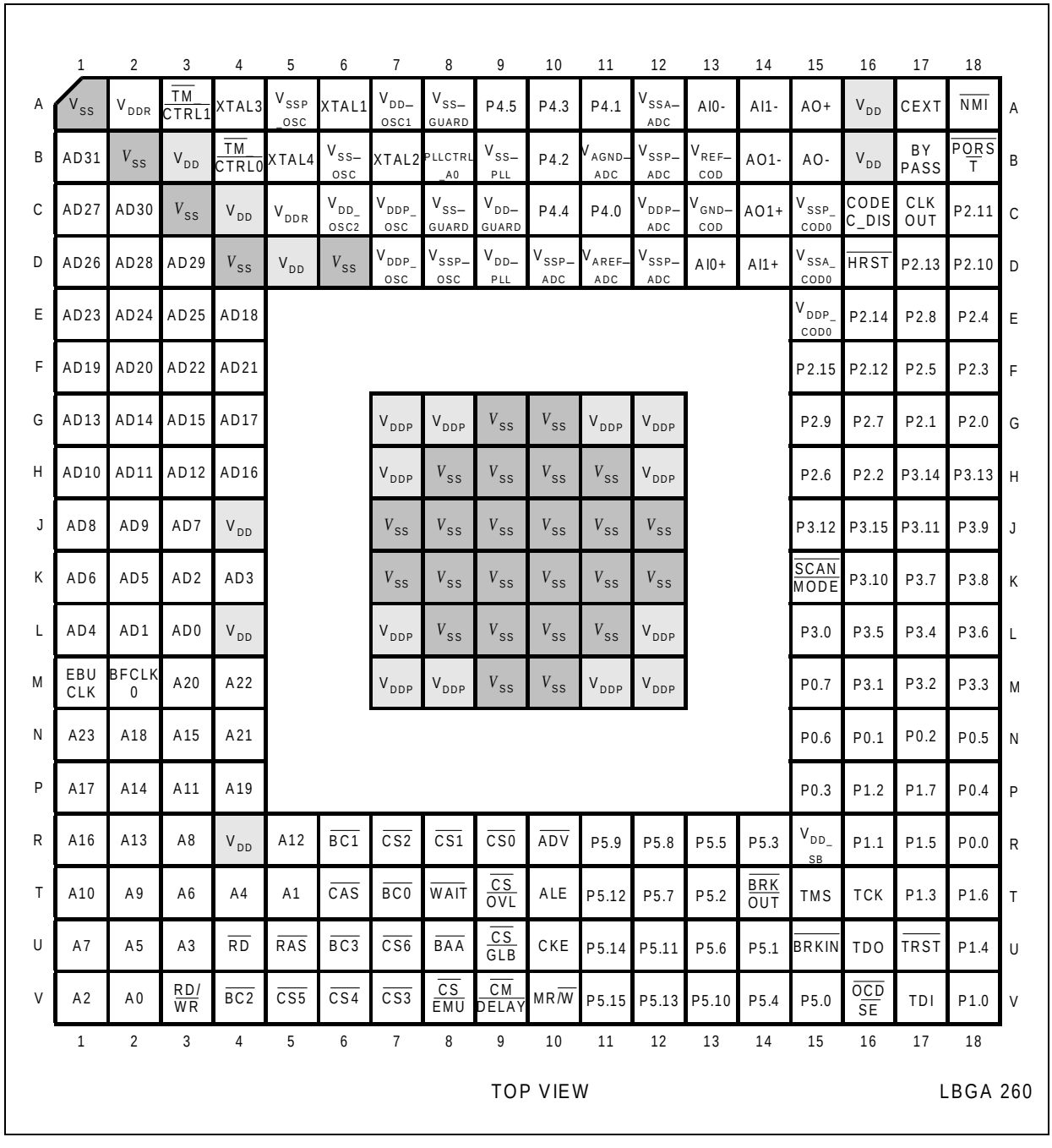


Figure 3 TC1920 Pinning

Preliminary

Pin List

Table 1 Pin Definitions and Functions

Symbol	Pad[1)]	BGA BALL	In/ Out[2)]	Functions
				External Bus Unit interface external address/data bus (multiplexed bus mode) or data bus (demultiplexed bus mode) for the EBU:
AD0	274	L3	I/O,s	Address/data bus / Data bus line 0
AD1	273	L2	I/O,s	Address/data bus / Data bus line 1
AD2	272	K3	I/O,s	Address/data bus / Data bus line 2
AD3	271	K4	I/O,s	Address/data bus / Data bus line 3
AD4	270	L1	I/O,s	Address/data bus / Data bus line 4
AD5	269	K2	I/O,s	Address/data bus / Data bus line 5
AD6	268	K1	I/O,s	Address/data bus / Data bus line 6
AD7	264	J3	I/O,s	Address/data bus / Data bus line 7
AD8	263	J1	I/O,s	Address/data bus / Data bus line 8
AD9	262	J2	I/O,s	Address/data bus / Data bus line 9
AD10	261	H1	I/O,s	Address/data bus / Data bus line 10
AD11	260	H2	I/O,s	Address/data bus / Data bus line 11
AD12	259	H3	I/O,s	Address/data bus / Data bus line 12
AD13	258	G1	I/O,s	Address/data bus / Data bus line 13
AD14	253	G2	I/O,s	Address/data bus / Data bus line 14
AD15	252	G3	I/O,s	Address/data bus / Data bus line 15
AD16	251	H4	I/O,s	Address/data bus / Data bus line 16
AD17	250	G4	I/O,s	Address/data bus / Data bus line 17
AD18	249	E4	I/O,s	Address/data bus / Data bus line 18
AD19	248	F1	I/O,s	Address/data bus / Data bus line 19
AD20	247	F2	I/O,s	Address/data bus / Data bus line 20
AD21	243	F4	I/O,s	Address/data bus / Data bus line 21
AD22	242	F3	I/O,s	Address/data bus / Data bus line 22
AD23	241	E1	I/O,s	Address/data bus / Data bus line 23
AD24	240	E2	I/O,s	Address/data bus / Data bus line 24
AD25	239	E3	I/O,s	Address/data bus / Data bus line 25
AD26	238	D1	I/O,s	Address/data bus / Data bus line 26
AD27	237	C1	I/O,s	Address/data bus / Data bus line 27
AD28	232	D2	I/O,s	Address/data bus / Data bus line 28
AD29	231	D3	I/O,s	Address/data bus / Data bus line 29
AD30	230	C2	I/O,s	Address/data bus / Data bus line 30
AD31	229	B1	I/O,s	Address/data bus / Data bus line 31

Table 1 Pin Definitions and Functions

Symbol	Pad[1)]	BGA BALL	In/ Out[2)]	Functions
				External Bus Unit interface (continued) external address bus for the EBU or chip select output lines.
A0	9	V2	I/O,s	Address bus line 0
A1	6	T5	I/O,s	Address bus line 1
A2	5	V1	I/O,s	Address bus line 2
A3	4	U3	I/O,s	Address bus line 3
A4	3	T4	I/O,s	Address bus line 4
A5	2	U2	I/O,s	Address bus line 5
A6	307	T3	I/O,s	Address bus line 6
A7	306	U1	I/O,s	Address bus line 7
A8	303	R3	I/O,s	Address bus line 8
A9	302	T2	I/O,s	Address bus line 9
A10	301	T1	I/O,s	Address bus line 10
A11	300	P3	I/O,s	Address bus line 11
A12	299	R5	I/O,s	Address bus line 12
A13	295	R2	I/O,s	Address bus line 13
A14	294	P2	I/O,s	Address bus line 14
A15	293	N3	I/O,s	Address bus line 15
A16	292	R1	I/O,s	Address bus line 16
A17	291	P1	I/O,s	Address bus line 17
A18	290	N2	I/O,s	Address bus line 18
A19	289	P4	I/O,s	Address bus line 19
A20	285	M3	I/O,s	Address bus line 20
A21	284	N4	I/O,s	Address bus line 21
A22	283	M4	I/O,s	Address bus line 22
A23	282	N1	I/O,s	Address bus line 23
$\overline{CS0}$	28	R9	O,u	Chip select output 0
$\overline{CS1}$	27	R8	O,u	Chip select output 1
$\overline{CS2}$	26	R7	O,u	Chip select output 2
$\overline{CS3}$	25	V7	O,u	Chip select output 3
$\overline{CS4}$	24	V6	O,u	Chip select output 4
$\overline{CS5}$	23	V5	O,u	Chip select output 5
$\overline{CS6}$	22	U7	O,u	Chip select output 6
$\overline{CSEMU}$	36	V8	O,u	Chip select for emulator region
$\overline{CSOVL}$	37	T9	O,u	Chip select for emulator overlay memory

Preliminary

Table 1 Pin Definitions and Functions

Symbol	Pad[1]	BGA BALL	In/ Out[2]	Functions
				External Bus Unit interface (continued) control bus for the EBU control lines.
$\overline{RD}$	11	U4	I/O,u	Read control line
RD/$\overline{WR}$	12	V3	I/O,u	Write control line
$\overline{ALE}$	45	T10	O,d	Address latch enable
$\overline{ADV}$	46	R10	O,u	Address valid output
$\overline{BC0}$	218	T7	I/O,u	Byte control line 0
$\overline{BC1}$	17	R6	I/O,u	Byte control line 1
$\overline{BC2}$	16	V4	I/O,u	Byte control line 2
$\overline{BC3}$	15	U6	I/O,u	Byte control line 3
$\overline{WAIT}$	32	T8	I/O,u	Wait input
$\overline{BAA}$	33	U8	O,u	Burst address advance output
EBUCLK	278	M1	O,d	External Bus Clock
BFCLK0	279	M2	O,d	Additional clock
$\overline{CSGLB}$	38	U9	O,u	Chip Select Global
$\overline{CMDELAY}$	39	V9	I,u	Command Delay
MR/$\overline{W}$	40	V10	O,u	Motorola-style Read/Write
$\overline{CKE}$	44	U10	O,d	Clock Enable
$\overline{RAS}$	13	U5	O,u	Row Address Strobe
$\overline{CAS}$	14	T6	O,u	Column Address Strobe
P0				Port 0 Port 0 serves as 8-bit general purpose I/O port, that can also be used for the codec digital signals. P0.[3:0] also serve as external interrupt inputs.
P0.0	94	R18	I/O	EXI0IN External interrupt input 0
P0.1	95	N16	I/O	EXI1IN Ext. interrupt input 1 / DATA_IN
P0.2	98	N17	I/O	EXI2IN Ext. interrupt input 2 / DATA_OUT
P0.3	102	P15	I/O	EXI3IN Ext. interrupt input 3 / MCLK
P0.4	103	P18	I/O	SCLK
P0.5	104	N18	I/O	LRCK
P0.6	105	N15	I/O	MUTE0
P0.7	106	M15	I/O	MUTE1

Preliminary

Table 1 Pin Definitions and Functions

Symbol	Pad[1)]	BGA BALL	In/ Out[2)]	Functions	
P1				Port 1 Port 1 is an 8-bit bidirectional general purpose I/O port which is also used as input/output for the GPTU1	
P1.0	83	V18	I/O	GPTU1.0	GPTU1 I/O line 0
P1.1	84	R16	I/O	GPTU1.1	GPTU1 I/O line 1
P1.2	85	P16	I/O	GPTU1.2	GPTU1 I/O line 2
P1.3	86	T17	I/O	GPTU1.3	GPTU1 I/O line 3
P1.4	87	U18	I/O	GPTU1.4	GPTU1 I/O line 4
P1.5	91	R17	I/O	GPTU1.5	GPTU1 I/O line 5
P1.6	92	T18	I/O	GPTU1.6	GPTU1 I/O line 6
P1.7	93	P17	I/O	GPTU1.7	GPTU1 I/O line 7
P2				Port 2 Port 2 is a 16-bit bidirectional general purpose I/O port which is also used as input/output for serial interfaces (CAN, J1850, IIC, ASC0, SSC)	
P2.0	131	G18	I/O	RXDCAN0	CAN 0 receiver input
P2.1	132	G17	I/O	TXDCAN0	CAN 0 transmitter output
P2.2	133	H16	I/O	RXDCAN1	CAN 1 receiver input
P2.3	137	F18	I/O	TXDCAN1	CAN 1 transmitter output
P2.4	138	E18	I/O	RXJ1850	SDLM receiver input
P2.5	139	F17	I/O	TXJ1850	SDLM transmitter output
P2.6	140	H15	I/O	SCL0	IIC Serial Port Clock line 0
P2.7	141	G16	I/O	SDA0	IIC Serial Port Data line 0
P2.8	142	E17	I/O	SCL1	IIC Serial Port Clock line 1
P2.9	143	G15	I/O	SDA1	IIC Serial Port Data line 1
P2.10	147	D18	I/O	RXD0	ASC0 receiver input/output
P2.11	148	C18	I/O	TXD0	ASC0 transmitter output
P2.12	149	F16	I/O	SCLK	SSC clock line
P2.13	150	D17	I/O	MRST	SSC master receive/slave transmit
P2.14	151	E16	I/O	MTSR	SSC master transmit/slave receive
P2.15	152	F15	I/O	PLL_CLC.LOCK	Monitoring of PLL_CLC.LOCK

Preliminary

Table 1 Pin Definitions and Functions

Symbol	Pad[1)]	BGA BALL	In/ Out[2)]	Functions
P3				Port 3 Port 3 is a 16-bit bidirectional general purpose I/O port which is also used as input/output for serial interfaces (ASC0 and ASC1), for timer (GPTU0) and ADC control lines
P3.0	107	L15	I/O	GPTU0.0 GPTU0 I/O line 0
P3.1	108	M16	I/O	GPTU0.1 GPTU0 I/O line 1
P3.2	109	M17	I/O	GPTU0.2 GPTU0 I/O line 2
P3.3	110	M18	I/O	GPTU0.3 GPTU0 I/O line 3
P3.4	115	L17	I/O	GPTU0.4 GPTU0 I/O line 4
P3.5	116	L16	I/O	GPTU0.5 GPTU0 I/O line 5
P3.6	117	L18	I/O	GPTU0.6 GPTU0 I/O line 6
P3.7	118	K17	I/O	GPTU0.7 GPTU0 I/O line 7
P3.8	119	K18	I/O	RXD1 ASC1 receiver input/output
P3.9	120	J18	I/O	TXD1 ASC1 transmitter output
P3.10	124	K16	I/O	RXD2 ASC2 receiver input/output
P3.11	125	J17	I/O	TXD2 ASC2 transmitter output OSCBYP latch-in input
P3.12	126	J15	I/O	ADCMUX0/EXI5IN/HWCFG0 ADC external mux control 0 / external interrupt input 5 / hardware configuration input 0 /
P3.13	127	H18	I/O	ADCMUX1/EXI6IN/HWCFG1 ADC external mux control 1 / external interrupt input 6 / hardware configuration input 1
P3.14	128	H17	I/O	ADCMUX2/EXI7IN/HWCFG2 ADC external mux control 2 / external interrupt input 7/ hardware configuration input 2
P3.15	129	J16	I/O	ADEXTIN ADC external trigger input

Preliminary

Table 1 Pin Definitions and Functions

Symbol	Pad[1]	BGA BALL	In/ Out[2]	Functions	
P4				Port 4 Port 4 provides the 6 analog input lines for the AD Converter (ADC).	
P4.0	190	C11	I	AIN0	Analog input 0
P4.1	191	A11	I	AIN1	Analog input 1
P4.2	192	B10	I	AIN2	Analog input 2
P4.3	193	A10	I	AIN3	Analog input 3
P4.4	194	C10	I	AIN4	Analog input 4
P4.5	195	A9	I	AIN5	Analog input 5
CODEC				CODEC	
AI0+	180	D13	I	CODEC 0 Non-Inverting Input	
AI0-	181	A13	I	CODEC 0 Inverting Input	
AO0+	169	A15	O	CODEC 0 Non-Inverting Output	
AO0-	165	B15	O	CODEC 0 Inverting Output	
AI1+	176	D14	I	CODEC 1 Non-Inverting Input	
AI1-	177	A14	I	CODEC 1 Inverting Input	
AO1+	170	C14	O	CODEC 1 Non-Inverting Output	
AO1-	172	B14	O	CODEC 1 Inverting Output	
CEXT	162	A17	I	Codec External Clock Input	
CODEC_DIS	163	C16	I	Codec Disable (power saving)	
DEBUG				DEBUG (OCDS/JTAG Control)	
$\overline{\text{TRST}}$	82	U17	I,d	Reset/module enable	
TCK	81	T16	I,u	JTAG clock input	
TDI	80	V17	I,u	Serial data input	
TDO[3]	76	U16	O	Serial data output	
TMS	75	T15	I,u	State machine control signal	
$\overline{\text{OCDSE}}$	73	V16	I,u	OCDS enable input	
$\overline{\text{BRKIN}}$	72	U15	I,u	OCDS break input	
$\overline{\text{BRKOUT}}$[3]	71	T14	O	OCDS break output	
Test				Test pins	
$\overline{\text{SCAN\_MODE}}$	114	K15	I	Scan Mode	
PLLCTRL_AO	202	B8	I	Control current of different analog stages	
TM_CTRL0	215	B4	I	Test Mode Control 0	
TM_CTRL1	216	A3	I	Test Mode Control 1	

Preliminary

Table 1 Pin Definitions and Functions

Symbol	Pad[1)]	BGA BALL	In/ Out[2)]	Functions
P5 TRACE [15:0]				Port 5 Trace Lines to output CPU or PCP2 OCDS level 2 trace signals
P5.0	70	V15	I/O	CPU or PCP2 trace output 0 / GPIO
P5.1	69	U14	I/O	CPU or PCP2 trace output 1 / GPIO
P5.2	68	T13	I/O	CPU or PCP2 trace output 2 / GPIO
P5.3	67	R14	I/O	CPU or PCP2 trace output 3 / GPIO
P5.4	63	V14	I/O	CPU or PCP2 trace output 4 / GPIO
P5.5	62	R13	I/O	CPU or PCP2 trace output 5 / GPIO
P5.6	61	U13	I/O	CPU or PCP2 trace output 6 / GPIO
P5.7	60	T12	I/O	CPU or PCP2 trace output 7 / GPIO
P5.8	59	R12	I/O	CPU or PCP2 trace output 8 / GPIO
P5.9	58	R11	I/O	CPU or PCP2 trace output 9 / GPIO
P5.10	54	V13	I/O	CPU or PCP2 trace output 10 / GPIO
P5.11	53	U12	I/O	CPU or PCP2 trace output 11 / GPIO
P5.12	52	T11	I/O	CPU or PCP2 trace output 12 / GPIO
P5.13	51	V12	I/O	CPU or PCP2 trace output 13 / GPIO
P5.14	48	U11	I/O	CPU or PCP2 trace output 14 / GPIO
P5.15	47	V11	I/O	CPU or PCP2 trace output 15 / GPIO
BYPASS	161	B17	I,d	PLL Bypass Control Input.
$\overline{\text{NMI}}$	160	A18	I,u	Non-Maskable Interrupt Input
$\overline{\text{HRST}}$	159	D16	I/O,u	Bidirectional Hardware Reset
$\overline{\text{PORST}}$	158	B18	I,u	Power-on Reset Input $\overline{\text{PORST}}$ must be active during power-up of the device
CLKOUT	156	C17	O	CPU Clock Output
XTAL1 XTAL2	208 207	A6 B7	I O	PLL/Oscillator Input/Output
XTAL3 XTAL4	214 213	A4 B5	I O	Real Time Clock Oscillator input/output (32 KHz)
V_{DD_OSC1}	206	A7	-	Main Oscillator Power Supply (1.8V)
V_{DD_OSC2}	212	C6	-	RTC Oscillator Power Supply (1.8V)
V_{SS_OSC}	211	B6	-	RTC & Main Oscillator Ground (1.8V)
V_{DDP_OSC}	205	D7	-	RTC & Main Oscillator Power Supply (3.3V)

Preliminary

Table 1 Pin Definitions and Functions

Symbol	Pad[1)]	BGA BALL	In/ Out[2)]	Functions
V_{DDP_OSC}	210	C7	-	RTC & Main Oscillator Power Supply (3.3V)
V_{SSP_OSC}	203	D8	-	RTC & Main Oscillator Ground (3.3V)
V_{SSP_OSC}	209	A5	-	RTC & Main Oscillator Ground (3.3V)
V_{DD_PLL}	198	D9	-	PLL Supply (1.8V)
V_{SS_PLL}	199	B9	-	PLL Ground (1.8V)
V_{DDP_ADC}	185	C12	-	ADC Port and Analog Part Power Supply (3.3V)
V_{SSP_ADC}	184	B12	-	ADC Port and Analog Part Ground (3.3V)
V_{SSP_ADC}	186	D12	-	ADC Port and Analog Part Ground (3.3V)
V_{SSP_ADC}	196	D10	-	ADC Port and Analog Part Ground (3.3V)
V_{SSA_ADC}	187	A12	-	ADC Analog Ground (3.3V)
V_{AREF_ADC}	189	D11	-	ADC Reference Voltage
V_{AGND_ADC}	188	B11	-	ADC Reference Ground
V_{DDP_COD0}	166	E15	-	Codec 0 Port and Analog Part Power Supply (3.3V)
V_{SSA_COD0}	167	D15	-	Codec 0 Analog Ground
V_{DDP_COD1}	175	E15	-	Codec 1 Port and Analog Part Power Supply (3.3V)
V_{SSA_COD1}	174	D15	-	Codec 1 Analog Ground
V_{SSP_COD0}	168	C15	-	Codec 0 Pad Ground (3.3V)
V_{SSP_COD1}	173	C15		Codec 1 Pad Ground (3.3V)
V_{REF_COD}	178	B13	-	Codec 0,1 Reference Voltage
V_{GND_COD}	179	C13	-	Codec 0,1 Reference Ground
V_{DDR}	217	A2	-	Stand-By SRAM Power Supply (1.8V)
V_{DDR}	224	C5	-	Stand-By SRAM Power Supply (1.8V)
V_{DD_GUARD}	200	C9	-	Guard Ring Supply (1.8V)
V_{SS_GUARD}	201	A8	-	Guard Ring Ground (1.8V)
V_{SS_GUARD}	204	C8	-	Guard Ring Ground (1.8V)
V_{DD_SB}	97	R15	-	Stand-By SRAM Battery Backed Stand-By Power Supply (1.8V)
V_{DDP}	[4)]		-	Port Pins Power Supply (3.3V)

Preliminary

Table 1 Pin Definitions and Functions

Symbol	Pad[1)]	BGA BALL	In/ Out[2)]	Functions
V_{DD}	5)		-	Core Power Supply (1.8V)
V_{SS}	6)		-	Ground for Core and Ports

1) The pin number describes the position of a signal on the silicon. The mapping of the pin number to the corresponding BGA ball is done according to the used package.

2) The notification ',u' after the input/output type defines an internal pull-up resistor. An internal pull-down resistor is indicated by ',d'. For the lines AD[31:0] and A[23:0], the type of the pull device can be selected 's'.

3) Output driver comparable to GPIO Medium Driver/Sharp Edge.

4) The BGA balls for the 3.3V port power supply are: G11, G12, G7, G8, H12, H7, L12, L7, M11, M12, M7, M8.

5) The BGA balls for the 1.8V core power supply are:
A16, B16, B3, C4, D5, J4, L4, R4.

6) The BGA balls for the digital ground are:
A1, B2, C3, D4, D6, G10, G9, H10, H11, H8, H9, J10, J11, J12, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L8, L9, M10, M9.

Preliminary

System Architecture and Control

32-Bit TriCore CPU

- 32-bit architecture with 4-GByte unified data, program and input/output address space
- Fast automatic context-switch
- Dual 16 x 16 Multiply-accumulate (MAC) unit
- Saturating integer arithmetic
- Register based design with multiple variable register banks
- Bit handling
- Packed data operations
- Zero overhead loop
- Precise exceptions
- Flexible power management

Instruction Set with High Efficiency:

- 16/32-bit instructions for reduced code size
- Little endian byte ordering with support for big and little endian byte ordering at bus interface
- Boolean, array of bits, character, signed and unsigned integer, integer with saturation, signed fraction, double word integers and IEEE-754 single precision floating-point data types
- Bit, 8-bit byte, 16-bit half word, 32-bit word and 64-bit double word data formats
- Powerful instruction set
- Flexible and efficient addressing mode for high code density

On-chip Code Memories

PMU Scratch-Pad SRAM (CSRAM):

The PMU memory consists of 24-KByte Code Scratchpad RAM (CSRAM) and 8-KByte Instruction Cache (ICACHE).

Address range of the CSRAM:

- D400 0000_H - D400 $5FFF_H$

Boot ROM (BROM):

The TC1920 contains 32 KByte of Boot ROM memory, which can be used for device operating mode initialization routines, bootstrap loader support or test functions.

The address range of the Boot ROM is:

- DFFF 8000_H – DFFF $FFFF_H$

Preliminary

On-chip Data Memories

DMU Scratch-Pad SRAM (DSRAM):

The DMU memory consists of 24-KByte Data Scratchpad RAM (DSRAM) and 8-KByte Data Cache (DCACHE).

Address range of the DSRAM:

- $D000\ 0000_H$ - $D000\ 5FFF_H$

Local Memory Bus Memory (LMBRAM):

Address range of the 64 KByte Local Memory Bus Memory:

- $C000\ 0000_H$ - $C000\ FFFF_H$ (in segment 12 for cached operation)
- $E800\ 0000_H$ - $E800\ FFFF_H$ (in segment 14 for non-cached operation)

FPI-Bus Data Memory (FPIDRAM):

The FPI-Bus Data Memory (FPIDRAM) is a 16-KByte static RAM located on the FPI-Bus. It contains two parts: FPIDRAM0 and FPIDRAM1. One half of it (FPIDRAM1) can be used for standby power operation.

Address range of the FPI Data Memory:

- $9FFF\ 8000_H$ - $9FFF\ BFFF_H$ (in segment 9 for cached operation)
- $BFFF\ 8000_H$ - $BFFF\ BFFF_H$ (in segment 11 for non-cached operation)

On-chip PCP Memories

PCP Code Memory (PCODE):

The address range of the 16 KByte PCP Code Memory (PCODE) is:

- $F002\ 0000_H$ - $F002\ 3FFF_H$

PCP Data Memory (PRAM):

The address range of the 4 KByte PCP Data Memory (PRAM) is:

- $F001\ 0000_H$ - $F001\ 0FFF_H$

Preliminary

System Control Unit (SCU)

The System Control Unit of the TC1920 basically handles all system control tasks. All these system functions are tightly coupled and therefore they are handled physically by one unit, the SCU. The system tasks of the SCU are:

- Clock Generation and Control
- Reset control
- Power Management control and wake-up
- Watchdog timer
- Trace port control
- Device identification
- Standby SRAM control
- External interrupt capability (8 sources)

System timer (STM)

The System Timer is designed for global system timing applications requiring both high precision and long range. It is used by the CPU for software operating system issues.

Features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Driven by clock, f_{STM} (normally identical with the system clock).
- Counting begins at power-on reset
- Continuous operation is not affected by any reset condition except power-on reset

Preliminary

External Bus Interface (EBU_LMB)

EBU_LMB is connected to the Local Memory Bus (LMB) of the TC1920 and also to the FPI Bus. EBU_LMB is always a slave on the LMB and a master/slave on the FPI bus.

Any LMB masters thus can access external memories or devices through EBU_LMB. Currently the maximum length of the bursts are according to the size of program and data cache lines, i.e. 8 x 32-bit words. Single transfers (non-burst) are supported for 8-bit, 16-bit and 32-bit wide access.

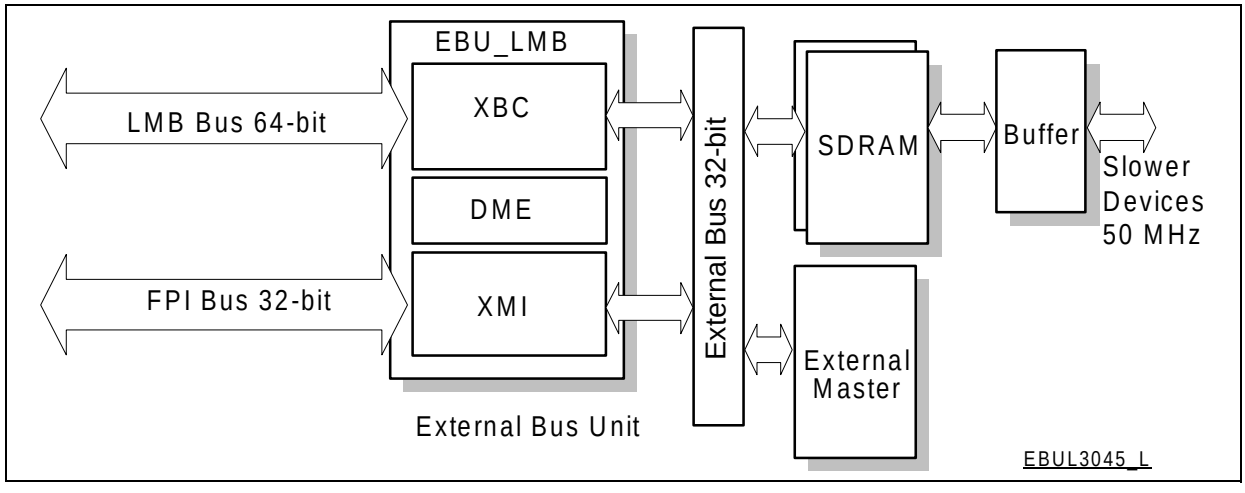


Figure 4 EBU_LMB block diagram

Features supported in EBU_LMB:

- Local Memory Bus (LMB 64-bit) support.
- External bus frequency: LMB frequency = 1:1 or 1:2 or 1:4.
- Highly programmable access parameters.
- Intel-style and Motorola-style peripheral/device support.
- SDRAM support (burst access, multibanking, precharge, refresh).
- 16- and 32-bit SDRAM data bus and support of 64, 128 and 256MBit devices.
- Burst flash support.
- Multiplexed access (address & data on the same bus) when SDRAM is not present on the External Bus.
- Data Buffering: Code Prefetch Buffer, Read/Write Buffer.
- External master arbitration (compatible to C166 and other TriCore devices).
- 8 programmable address regions (1 dedicated for emulator).
- Little-endian and Big-endian support.
- $\overline{\text{CSGLB}}$ signal, dedicated pin, bit programmable to combine one or more $\overline{\text{CS}}$ lines, for buffer control.
- $\overline{\text{RMW}}$ signal reflecting a read-modify-write action.
- Signal for controlling data flow of slow-memory buffer.
- Slave unit for external (off-chip) master to access devices on the FPI bus.
- Master unit for FPI master to access external (off-chip) devices.
- Data Mover Engine.

Preliminary

Interrupt System

- Flexible interrupt prioritizing scheme with 256 interrupt priority levels
- Fast interrupt response
- Service requests are serviced by the CPU or by the PCP (two independent interrupt buses, that can be selected by each interrupt source)

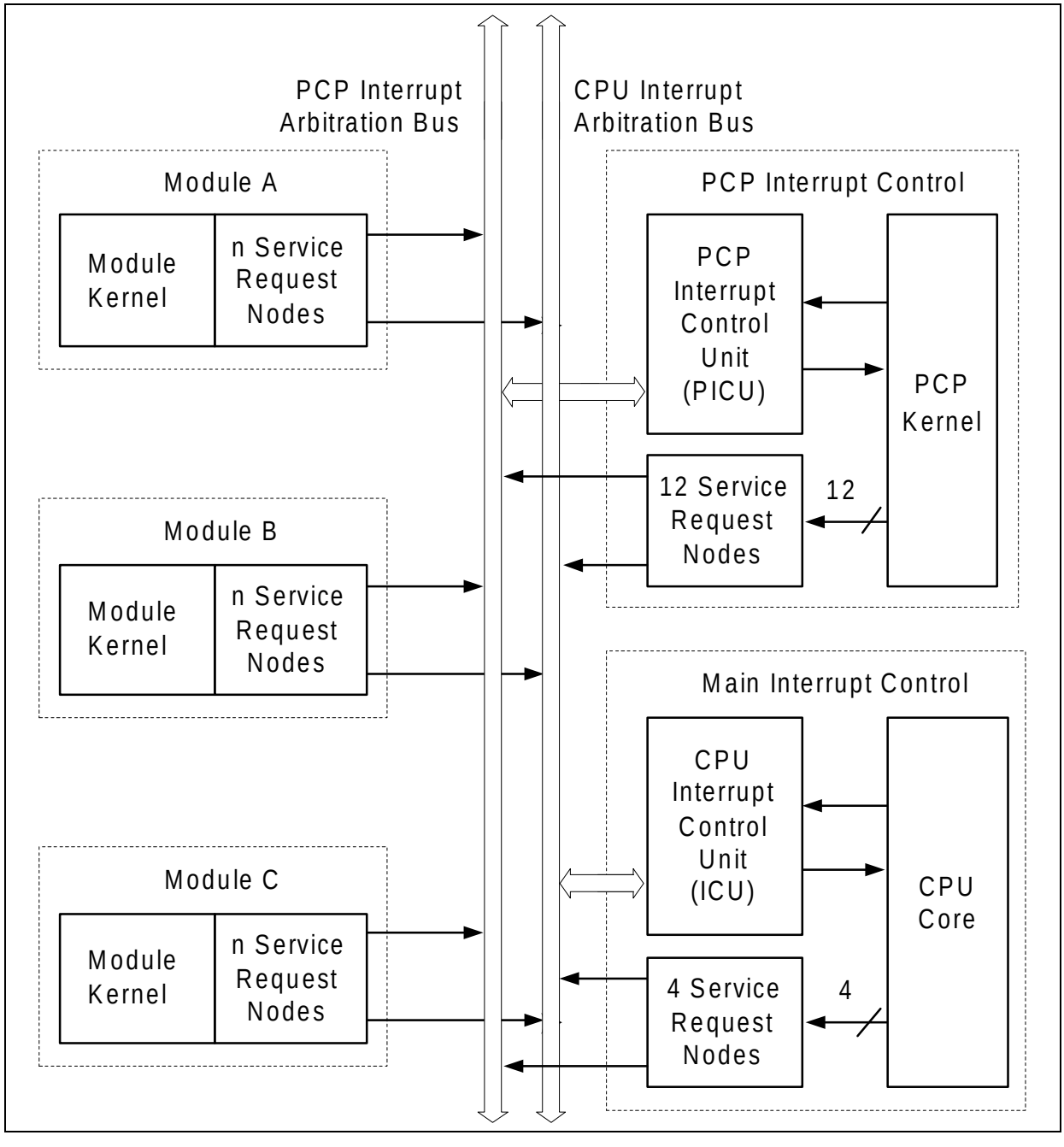


Figure 5 Block Diagram Interrupt System

Peripheral Control Processor (PCP)

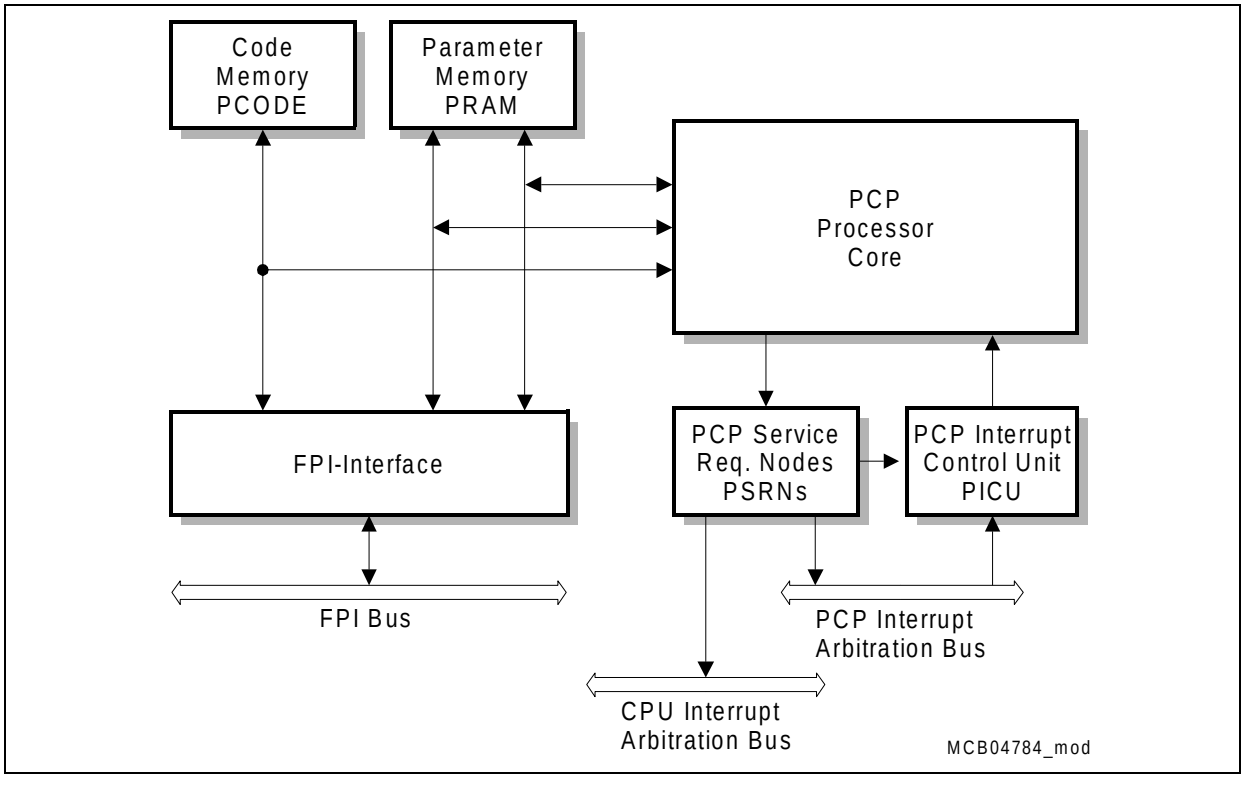


Figure 6 PCP block diagram

The PCP is designed to work in partnership with a host CPU and performs many of the tasks that would conventionally be performed by CPU interrupt service routines or a DMA controller. The PCP off-loads the host CPU from most of the time critical interrupts, easing the implementation of systems based on operating systems.

In principle the PCP may be considered to be a conventional processor which only executes code in response to interrupt service requests (i.e. has no processing which is not at interrupt level). It has an architecture which efficiently supports DMA type of bus transactions to / from arbitrary devices and memory addresses and also some reasonable computational capabilities. Whenever the PCP responds to a PCP interrupt request (which has a specific interrupt priority level) it will use a register set ("context") specific to that individual interrupt level and will also generally execute code which is also specific to that interrupt level. For this reason the term "Channel" will be used throughout the remainder of this document to refer to all PCP resources associated with a particular PCP interrupt level.

The architecture is flexible enough to allow the implementation of a subset of the commands/instructions as a simple DMA controller.

The PCP has a Harvard architecture (i.e. separate code and data memory spaces). Any FPI bus master (including the PCP itself) can access both PCP code (PCODE) and data (PRAM) memory via the FPI bus.

Preliminary

FPI Bus

The Flexible Peripheral Interconnect Bus is designed with the requirements of high-performance Systems-on-Chip in mind.

Key Features:

- Core independent
- Multi-master capability
- Demultiplexed operation
- Clock synchronous
- Peak transfer rate of up to 200 MBytes/s (@ 50 MHz bus clock)
- Address and data bus scalable (32 bit address bus, 32 bit data bus)
- 8-/16- and 32 bit data transfers
- Broad range of transfer types from single to multiple data transfers
- Burst transfer capability
- EMI and power consumption minimized

LMB-Bus

The Local Memory Bus is a synchronous, pipelined, split bus with variable block size transfer support. All signals relate to the positive clock edge.

The protocol supports 8,16,32 & 64 bits single beat transactions and variable length 64 bits block transfers.

Key Features:

The LMB provides the following features:

- Optimized for high speed and high performance
- 32 bit address, 64 bit data busses
- Central simple per cycle arbitration
- Slave controlled wait state insertion
- Address pipelining (max. depth - 2)
- Split transactions
- Variable block length - 2, 4 or 8 beats of 64 bit data

Preliminary

On-Chip Debug System (OCDS)

The TC1920 architecture is supporting OCDS level 1 and 2.

Level	Run Time Control	System access via		Basic PC trace
		JTAG	Trace bus	
1	Yes	Yes	No	No
2	Yes	Yes	Yes	Yes

Table 2 Core-related and System Control Modules

Module	Address Range	I/O Lines	Interrupt Nodes
TriCore CPU Slave Registers (CPS)	F7E0 FF00$_H$ - F7E0 FFFF$_H$	-	CPU_SRC0..3 CPU_SRCSB
Memory Management[1] Unit (MMU)	F7E1 8000$_H$ - F7E1 80FF$_H$	-	-
Segment Protection Registers[1]	F7E1 C000$_H$ - F7E1 C0FF$_H$	-	-
Core Debug[1] (Core OCDS)	F7E1 FD00$_H$ - F7E1 FDFF$_H$	-	-
TriCore CPU[1] SFR, GPR	F7E1 FE00$_H$ - F7E1 FFFF$_H$	-	-
Program Memory Unit[2] (PMU)	F87F FD00$_H$ - F87F FDFF$_H$	-	-
Data Memory Unit[2] (DMU)	F87F FC00$_H$ - F87F FCFF$_H$	-	-
Peripheral Control Processor (PCP)	F000 3F00$_H$ - F000 3FFF$_H$	-	PCP_SRC0..11
External Bus Unit (EBU)	F800 0000$_H$ - F800 03FF$_H$	AD[31:0], A[23:0], 27 control lines	-
System Control Unit (SCU)	F000 0000$_H$ - F000 00FF$_H$	4 XTAL, $\overline{\text{PORST}}$, $\overline{\text{HRST}}$, 8 EXIN, $\overline{\text{NMI}}$, 4 test, CLKOUT, BYPASS	EXI_SRC0..4 NMI[3]
FPI Bus Control Unit (BCU)	F000 0200$_H$ - F000 02FF$_H$	-	BCU_SRC

Preliminary

Table 2 Core-related and System Control Modules (cont'd)

Module	Address Range	I/O Lines	Interrupt Nodes
LMB Bus Control Unit (LCU)	F87F FE00$_H$ - F87F FEFF$_H$	-	LCU_SRC
LMB to FPI Bus Bridge (LFI)	F87F FF00$_H$ - F87F FFFF$_H$	-	-
Port Control (Ports 0, 1, 2, 3, 5)	F000 2800$_H$ - F000 2CFF$_H$	P0 (7), P1(7), P2(15), P3(15), P5(15)	-
Debug Support (JTAG, OCDS)	F000 0400$_H$ - F000 04FF$_H$	$\overline{TRST}$, TCK, TDI, TDO, TMS, $\overline{OCDSE}$, $\overline{BRKIN}$, $\overline{BRKOUT}$, 16 trace outputs	-

1) This address range is also accessed via the CPS by the FPI bus.

2) This address range is accessed via the LMB.

3) The NMI is directly connected to the core (no SRC) and always acts on the highest priority. It is used as highest priority interrupt for the NMI input, the watchdog, the PLL and for wake-up via the RTC or via the EXIx inputs.

On-Chip Peripheral Units

The TC1920 offers several on-chip peripheral units such as serial controllers, timer units, AD converter and Codec interface. Within the TC1920 all these peripheral units are connected to the TriCore CPU/system via the FPI (Flexible Peripheral Interconnect) Bus. Several IO lines on the TC1920 ports are reserved for these peripheral units to communicate with the external world.

Peripheral Units of the TC1920:

- Three Asynchronous/Synchronous Serial Channels with baudrate generator, parity, framing and overrun error detection, IrDA mode, FIFO buffers.
- One High Speed Synchronous Serial Channels with programmable data length and shift direction
- TwinCAN Module with two interconnected CAN nodes for high efficiency data handling via FIFO buffering and gateway data transfer
- Serial Data Link Module compliant to SAE Class B J1850 specification
- IIC module with connection to 2 external busses
- 2 multi-functional General Purpose Timer Units with three 32-bit timer/counter
- One Analog-to-Digital Converter Units with 8-bit, 10-bit, or 12-bit resolution and 6 analog inputs
- Dual channel Codec interface
- GPIO blocks

Table 3 Peripheral Modules

Module	Address Range	I/O Lines	Interrupt Nodes
Asynchronous Serial Channel 0 (ASC0)	$F000\ 0A00_H$ - $F000\ 0AFF_H$	RDX0, TDX0	ASC0_TSRC ASC0_RSRC ASC0_ESRC ASC0_TBSRC
Asynchronous Serial Channel 1 (ASC1)	$F000\ 0B00_H$ - $F000\ 0BFF_H$	RDX1, TDX1	ASC1_TSRC ASC1_RSRC ASC1_ESRC ASC1_TBSRC
Asynchronous Serial Channel 2 (ASC2)	$F000\ 0C00_H$ - $F000\ 0CFF_H$	RDX2, TDX2	ASC2_TSRC ASC2_RSRC ASC2_ESRC ASC2_TBSRC
Synchronous Serial Channel (SSC)	$F000\ 0800_H$ - $F000\ 08FF_H$	SCLK, MRST, MTSR	SSC_TSRC SSC_RSRC SSC_ESRC
Inter-IC Bus (IIC)	$F000\ 0500_H$ - $F000\ 05FF_H$	SCL[1:0], SDA[1:0]	IIC_XP0SRC IIC_XP1SRC IIC_XP2SRC
Real Time Clock (RTC)	$F000\ 0100_H$ - $F000\ 01FF_H$	-	RTC_SRC
System Timer Unit (STM)	$F000\ 0300_H$ - $F000\ 03FF_H$	-	-
General Purpose Timer 0 (GPTU0)	$F000\ 0700_H$ - $F000\ 07FF_H$	GPTU0[7:0]	GPTU0_SRC0..7
General Purpose Timer 1 (GPTU1)	$F000\ 0600_H$ - $F000\ 06FF_H$	GPTU1[7:0]	GPTU1_SRC0..7
CAN (TwinCAN)	$F010\ 0000_H$ - $F010\ 0BFF_H$	RXDCAN[1:0], TXDCAN[1:0]	CAN_SRC0..7
SDLM (J1850)	$F000\ 2600_H$ - $F000\ 26FF_H$	RXJ1850, TXJ1850	SDLM_SRC0..1

Table 3 Peripheral Modules (cont'd)

Module	Address Range	I/O Lines	Interrupt Nodes
Speech Interface (Codec)	F000 2400_H - F000 $24FF_H$	2*2 analog IN, 2*2 analog OUT, CEXT, CODEC_DIS	CODEC_SRC0..5
Analog to Digital Converter (ADC)	F000 2200_H - F000 $23FF_H$	AIN[5:0] = P4, ADEMUX[2:0], ADEXTIN	ADC_SRC0..3

Asynchronous/Synchronous Serial Interfaces (ASC 0/1/2)

The Asynchronous/Synchronous Serial Interface ASC provides serial communication between the TriCore and other microcontrollers, microprocessors or external peripherals. The implementation is held parametrizable in order to allow the usage of parallel busses of different width and with different protocols.

Features:

- Full duplex asynchronous operating modes
  - 8- or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baudrate from 3.125 MBaud to 0.74 Baud (@ 50 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baudrate from 6.25 MBaud to 637 Baud (@ 50 MHz module clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - on a transmitter buffer empty condition
  - on a transmit last bit of a frame condition
  - on a receiver buffer full condition
  - on an error condition (frame, parity, overrun error)
- Support for IrDA
- Automatic Baudrate Detection
- 8 Byte FIFO

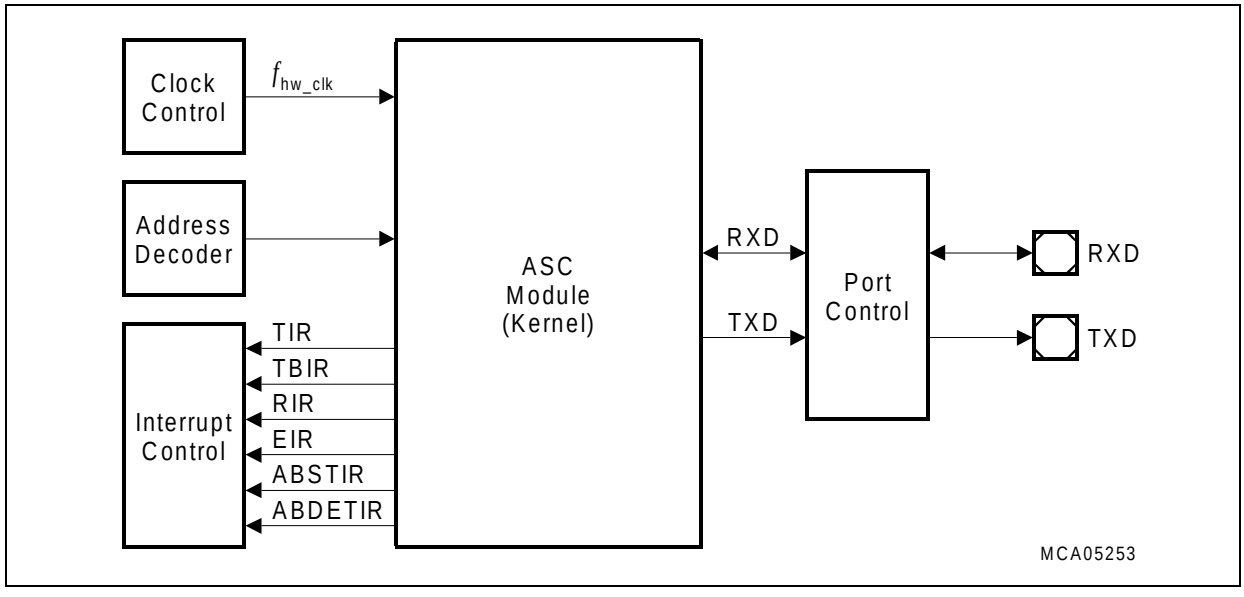


Figure 7 ASC Interface Diagram

Preliminary

High-Speed Synchronous Serial Interface (SSC)

The High Speed Synchronous Serial Interface SSC provides serial communication between microcontrollers, microprocessors or external peripherals. The SSC supports full-duplex and half-duplex synchronous communication up to 25 MBaud (@ 50 MHz module clock). The serial clock signal can be generated by the SSC itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A 16-bit baud rate generator provides the SSC with a separate serial clock signal.

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Flexible data format
  - Programmable number of data bits : 2 to 16 bit
  - Programmable shift direction : LSB or MSB shift first
  - Programmable clock polarity : idle low or high state for the shift clock
  - Programmable clock/data phase : data shift with leading or trailing edge of SCLK
- Maximum baudrates: 25 MBaud in Master, 12.5 in Slave mode (@ 50 MHz module clock)

Interrupt generation
  - on a transmitter empty condition
  - on a receiver full condition
  - on an error condition (receive, phase, baudrate, transmit error)
- Three pin interface

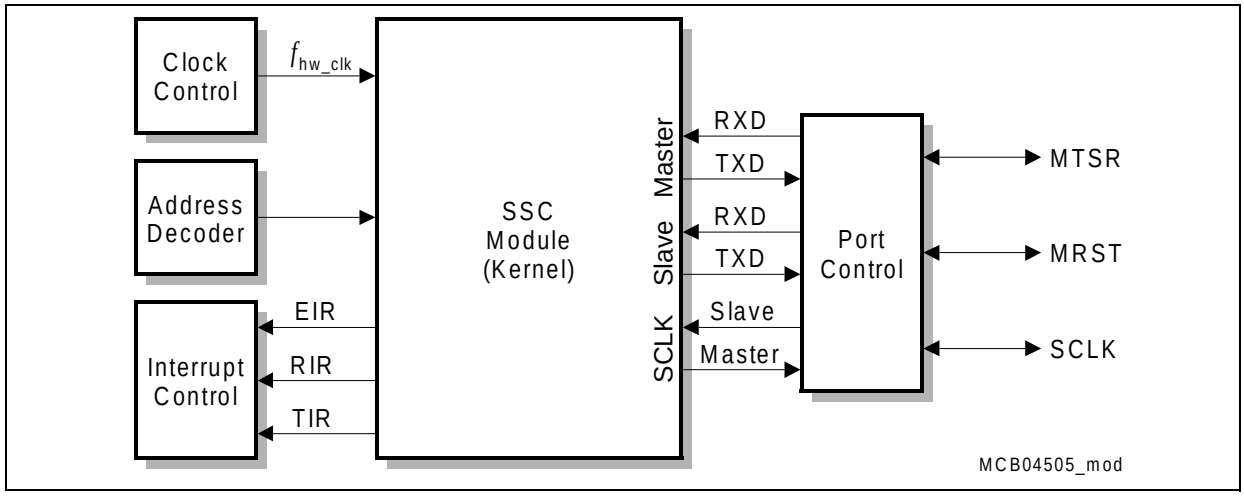


Figure 8 SSC Interface Diagram

Preliminary

Inter-IC Interface (IIC)

IIC supports a certain protocol to allow devices to communicate directly with each other via two wires. One line is responsible for clock transfer and synchronization (SCL), the other is responsible for the data transfer (SDA).

The on-chip IIC Bus module connects the platform buses to other external controllers and/or peripherals via the two-line serial IIC interface. The IIC Bus module provides communication at data rates of up to 400 kBit/s and features 7-bit addressing as well as 10-bit addressing. This module is fully compatible to the IIC bus protocol.

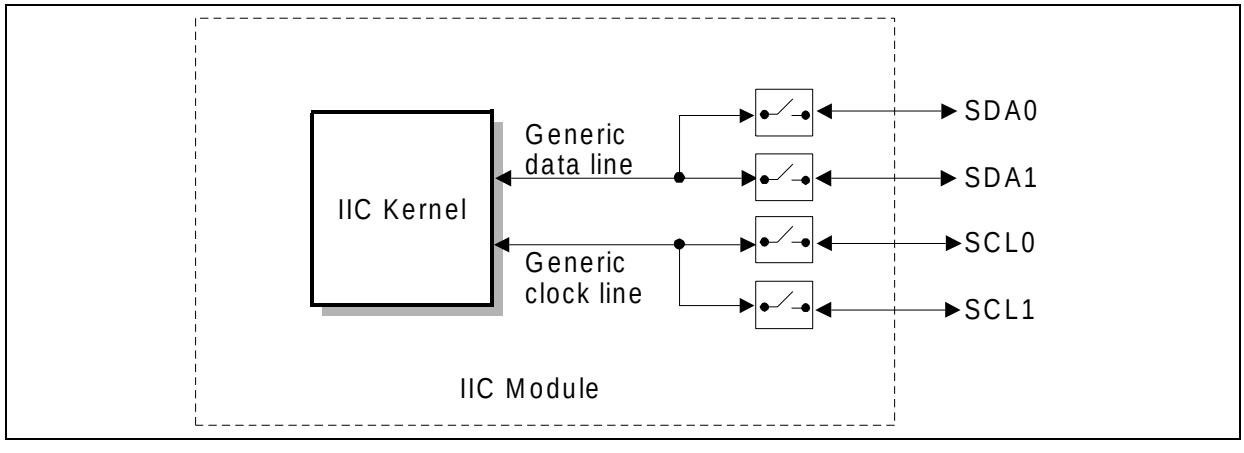


Figure 9 IIC Bus Line Connections

The module can operate in three different modes:

Master mode, where the IIC controls the bus transactions and provides the clock signal.

Slave mode, where an external master controls the bus and provides the clock signal.

Multimaster mode, where several masters can be connected to the bus, i.e. the IIC can be master or slave.

The module unloads the CPU of low level tasks like:

- (De)Serialization of bus data.
- Generation of start and stop conditions.
- Monitoring the bus lines in slave mode.
- Evaluation of the device address in slave mode.
- Bus access arbitration in multimaster mode.

IIC Features:

- Extended buffer allows up to 4 send/receive data bytes to be stored.
- Selectable baud rate generation.
- Support of standard 100 kBaud and extended 400 kBaud data rates.
- Operation in 7-bit addressing mode or 10-bit addressing mode.
- Flexible control via interrupt service routines or by polling.
- Dynamic access to up to 2 physical IIC busses.

Preliminary

CAN Interface (TwinCAN)

Figure 10 shows a global view of the functional blocks of the TwinCAN module.

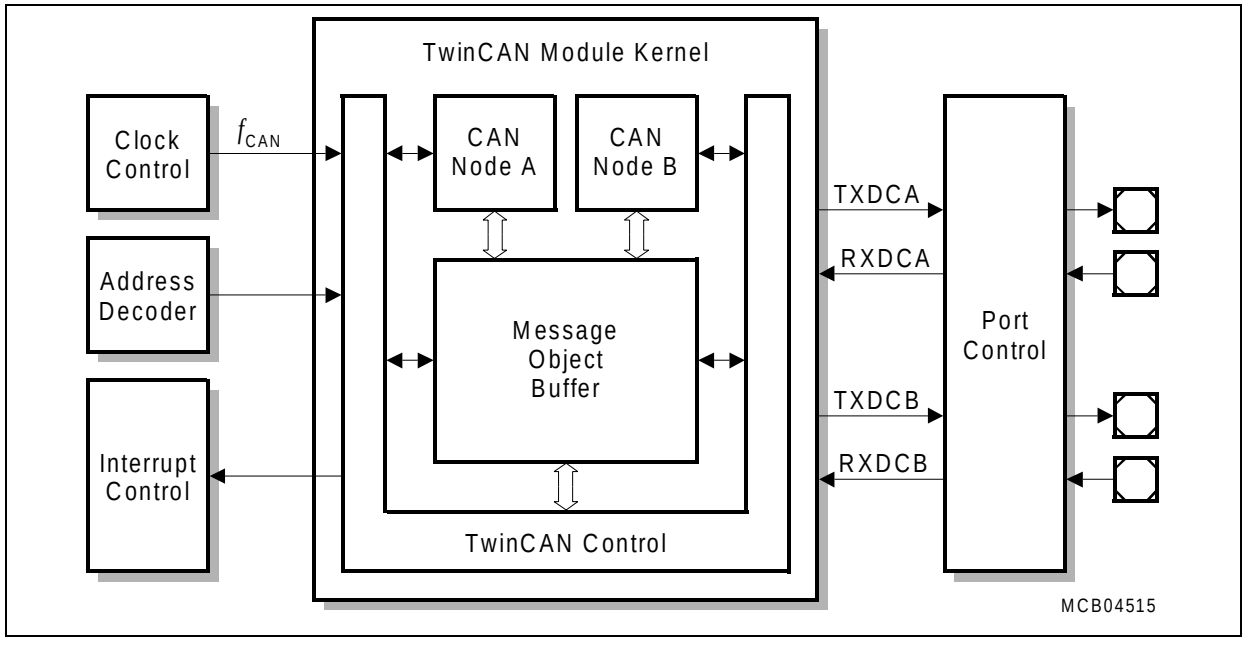


Figure 10 General Block Diagram of the TwinCAN Interfaces

TwinCAN Features:

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Full-CAN functionality: 32 message objects can be individually
  - assigned to one of the two CAN nodes,
  - configured as transmit or receive object,
  - participate in a 2,4,8,16 or 32 message buffer with FIFO algorithm,
  - setup to handle frames with 11 bit or 29 bit identifiers,
  - provided with programmable acceptance mask register for filtering,
  - monitored via a frame counter,
  - configured to Remote Monitoring Mode.
- Up to eight individually programmable interrupt nodes can be used.
- CAN Analyzer Mode for bus monitoring is implemented.

The TwinCAN module has four IO lines. The TwinCAN module is further supplied by a clock control, interrupt control, address decoding, and port control logic.

Preliminary

The CAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 part B (active). Each of the two Full-CAN nodes can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share the TwinCAN module's resources in order to optimize the CAN bus traffic handling and to minimize the CPU load. The flexible combination of Full-functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the increased number of message objects permit precise and comfortable CAN bus traffic handling.

Depending on the application, each of the 32 message objects can be individually assigned to one of the two CAN nodes. Gateway functionality allows automatic data exchange between two separate CAN bus systems, which reduces CPU load and improves the real time behavior of the entire system.

The bit timings for both CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connect each CAN node to a bus transceiver.

Preliminary

Serial Data Link Module (J1850)

Figure 11 shows a global view of the functional blocks of the J1850 interface.

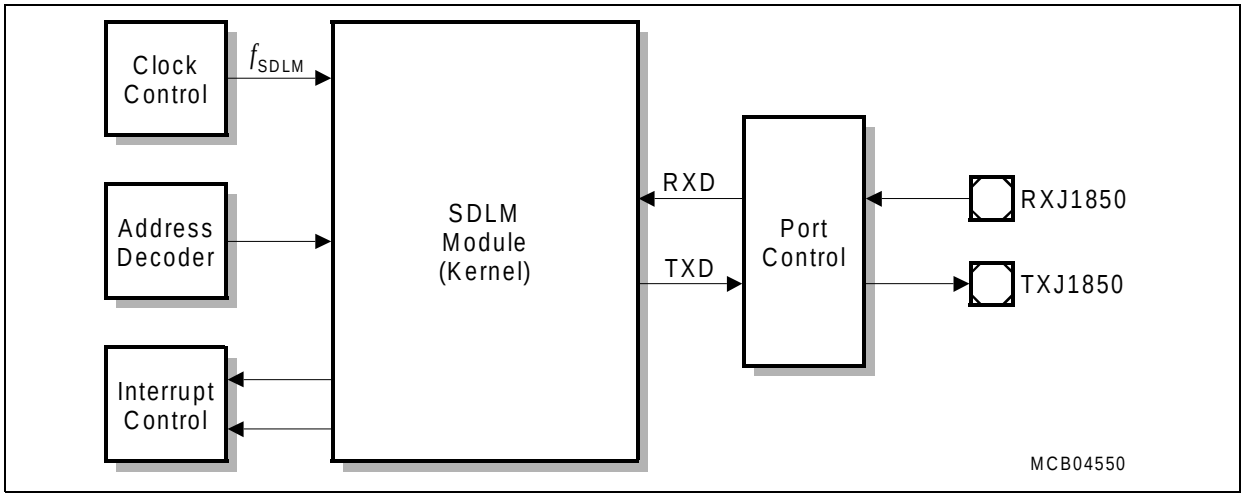


Figure 11 General Block Diagram of the SDLM Interface

The J1850 module communicates with the external world via two I/O lines, the J1850 bus. The RXD line is the receive data input signal and TXD is the transmit data output signal. The Serial Data Link Module provides serial communication to a J1850 based serial bus. J1850 bus transceivers have to be implemented externally in a system. The J1850 module is conform to the SAE Class B J1850 specification and compatible to class 2 protocol.

General SDLM Features:

- Compliant to SAE Class B J1850 specification
- Full support of GM class 2 protocol
- Variable Pulse Width (VPW) format with 10.4 kBaud
- High speed receive/transmit 4x mode with 41.6 kBaud
- Digital noise filter
- Power save mode and automatic wake up upon bus activity
- Support of single byte headers or consolidated headers
- CRC generation & check
- Support of block mode for receive and transmit

Data Link Operation Features:

- 11 bytes transmit buffer
- Double buffered 11 bytes receive buffer
- Support of In-frame response (IFR) types 1,2,3
- Advanced interrupt handling for RX, TX and error conditions
- All interrupt sources can be enabled/disabled individually
- Support of automatic IFR for types 1,2 for three byte consolidated headers

Preliminary

Timer Units (GPTU 0/1)

Figure 12 shows a global view of all functional blocks of one GPTU module.

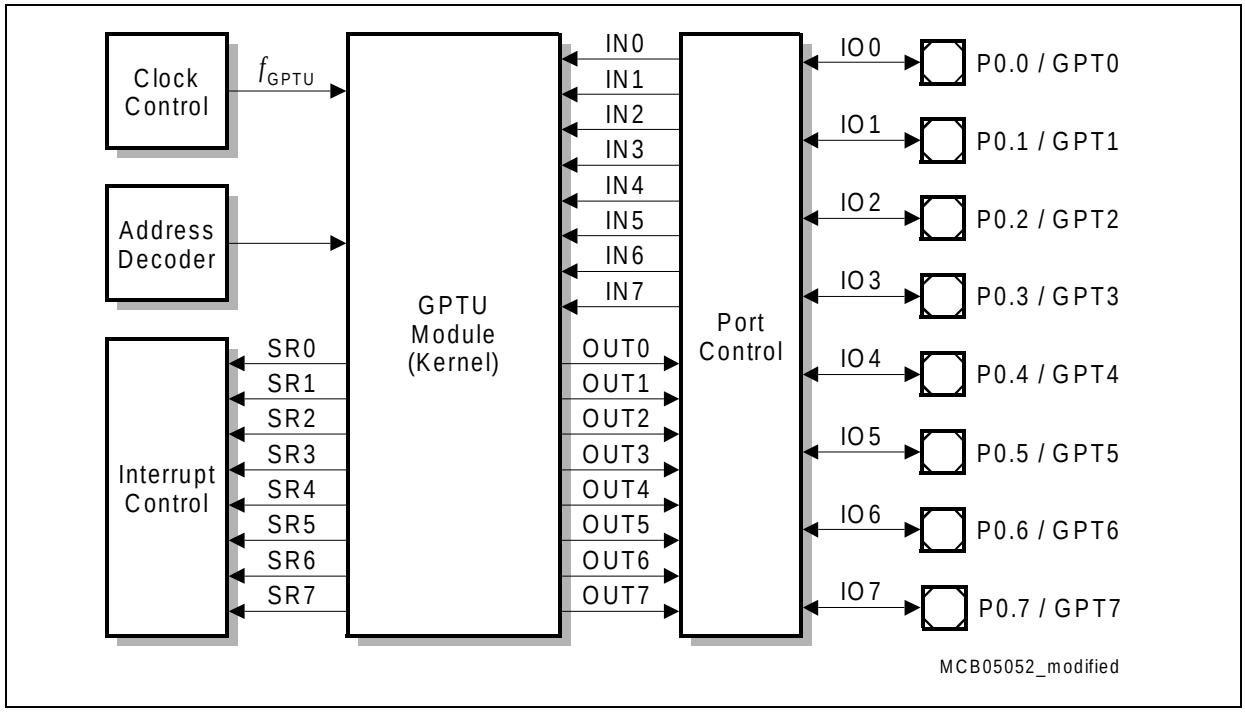


Figure 12 General Block Diagram of the GPTU Interface

The GPTU consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. The GPTU communicates with the external world via eight inputs and eight outputs.

The three timers of the GPTU module T0, T1, and T2, can operate independently from each other, or can be combined:

General Features:

- All timers are 32-bit precision timers with a maximum input frequency of $f_{GPTU}/2$.
- Events generated in T0 or T1 can be used to trigger actions in T2
- Timer overflow or underflow in T2 can be used to clock either T0 or T1
- T0 and T1 can be concatenated to form one 64-bit timer

Features of T0 and T1:

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers
- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Two input pins can determine a count option

Preliminary

Features of T2:

- Optionally count up or down
- Operating modes:
  - Timer
  - Counter
  - Incremental Interface Mode
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions.
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins
- T2 events are freely assignable to the service request nodes.

Preliminary

Analog to Digital Converter (ADC)

Figure 13 shows a global view of the ADC module kernel with the module specific interface connections.

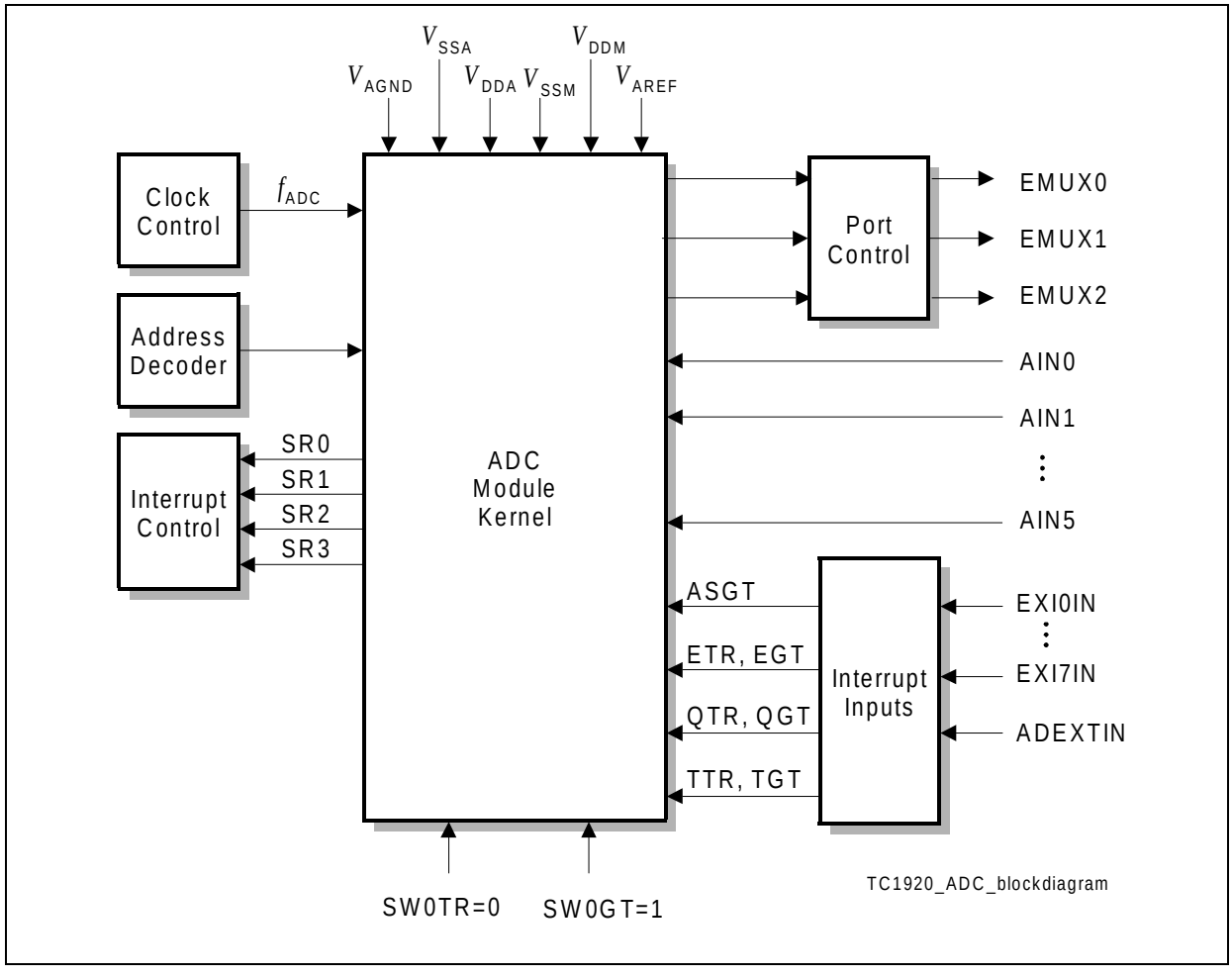


Figure 13 General Block Diagram of the ADC module

The on-chip ADC module of the TC1920 is an analog to digital converter with 8-bit, 10-bit or 12-bit resolution including sample & hold functionality. The A/D converter operates by the method of the successive approximation. A multiplexer selects between up to 6 analog input channels. Conversion requests are generated either under software control or by hardware. An automatic self-calibration adjusts the ADC module to changing temperatures or process variations.

Preliminary

Features:

The following functionality has been implemented in the on chip ADC module to fulfill the enhanced requirements of embedded control applications:

- 8-bit, 10-bit, 12-bit A/D Conversion
- Successive approximation conversion method
- Total Unadjusted Error (TUE) of ±2 LSB @ 10-bit resolution
- Integrated sample and hold functionality
- 6 analog input channels
- Dedicated control and status registers for each analog channel
- Flexible conversion request mechanisms
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Flexible ADC module service request control unit
- Automatic control of external analog multiplexer
- Equidistant samples initiated by timer
- External trigger inputs for conversion requests
- Power reduction and clock control feature

Real Time Clock Unit RTC

The Real Time Clock (RTC) module is basically an independent timer chain and counts clock ticks. The base frequency of the RTC can be programmed via a reload counter. The RTC can work fully asynchronous to the system frequency and is optimized on low power consumption.

Features:

The RTC serves different purposes:

- Absolute system clock to determine the current time and date
- Cyclic time based interrupt
- Alarm interrupt for wake up on a defined time
- 48-bit timer for long term measurements

Preliminary

Codec Interface

The speech A/D and D/A converters (called codec) is designed for telephone and speech recognition quality. They can be used for microphone / earpiece applications. The TC1920 configuration implements a dual channel speech codec connected to the FPI bus.

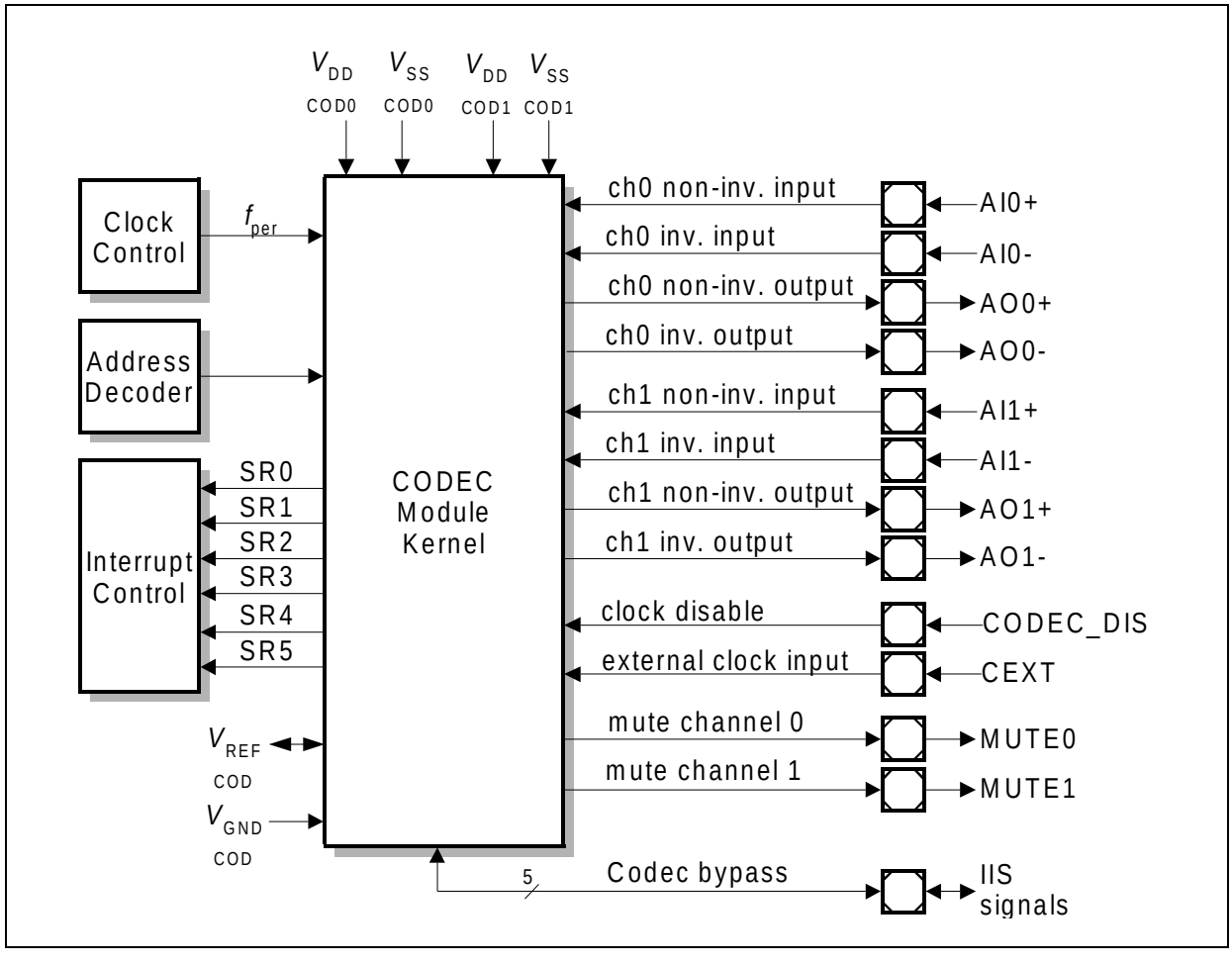


Figure 14 General Codec Overview

General Purpose I/Os (GPIO)

- Push/pull output drivers
- 3.3 Volt operation for GPIO
- Programmable pull-up/-down devices at all pins
- Optional Open Drain Output Mode

Preliminary

Power Supply

Figure 15 shows the TC1920 power supply concept, where certain logic modules are individually supplied with power. In this way, the noise margin is improved in the especially sensitive modules, like the A/D converter and the CODEC.

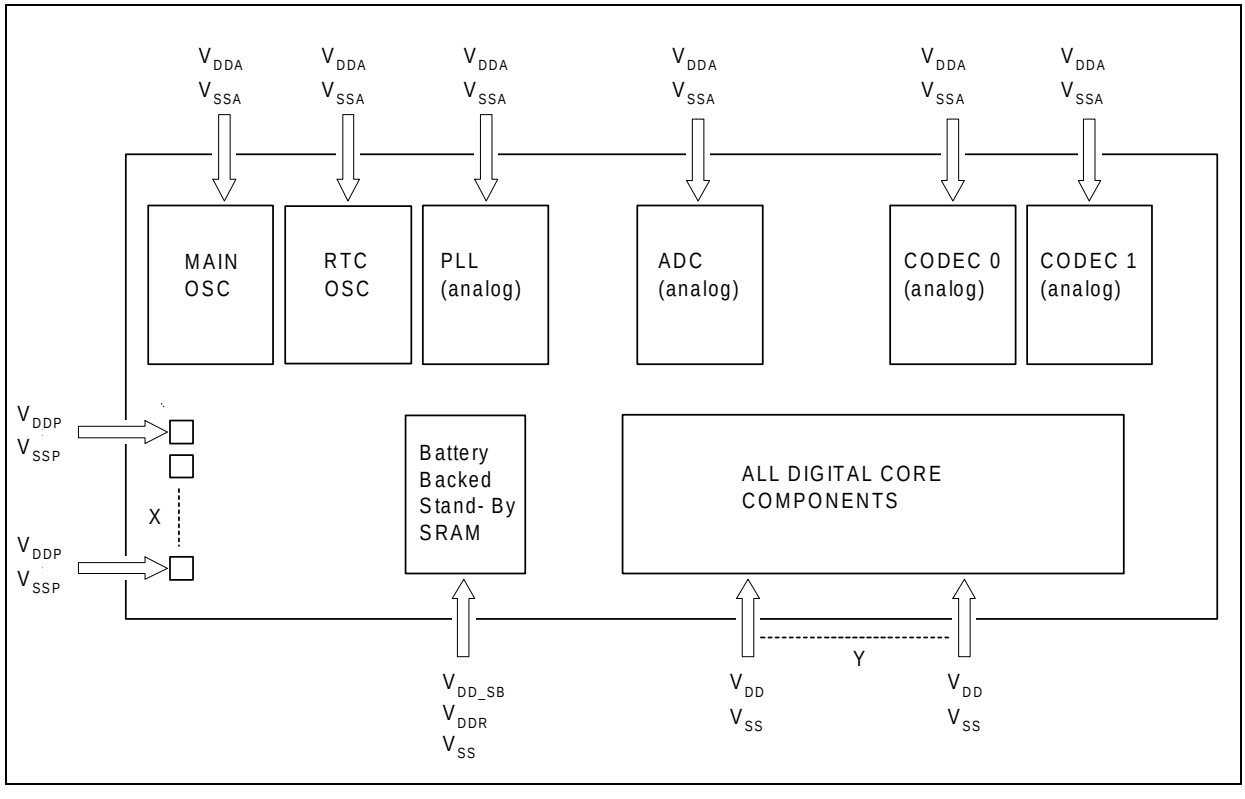


Figure 15 TC1920 Power Supply Concept

Preliminary

Power-Up Sequence

During Power-Up reset pin $\overline{\text{PORST}}$ has to be held active until both power supply voltages have reached at least their minimum values.

During the Power-Up time (rising of the supply voltages from 0 to their regular operating values) it has to be ensured, that the core V_{DD} power supply reaches its operating value first, and then the GPIO V_{DDP} power supply. During the rising time of the core voltage it must be ensured that $0 < V_{DD}-V_{DDP} < 0.5$ V.

During power-down, the core and GPIO power supplies V_{DD} and V_{DDP} respectively, have to be switched off until all capacitances are discharged to zero, before the next power-up.

Note: The states of the pins are undefined when only the port voltage V_{DDP} is on.

Preliminary

ID Register Table

Table 4 List of TC1920 ID registers

Short Name	Description	Address	Value
SCU_ID	SCU Identification Register	F000 0008$_H$	0019 C002$_H$
MANID	Manufacturer Identification Register	F000 0070$_H$	0000 1820$_H$
CHIPID	Chip Identification Register	F000 0074$_H$	0000 8902$_H$
RTID	Redesign Tracing Identification Register	F000 0078$_H$	0000 0000$_H$
RTC_ID	RTC Module Identification Register	F000 0108$_H$	0000 5A04$_H$
BCU_ID	BCU Identification Register	F000 0208$_H$	0000 6A06$_H$
STM_ID	System Timer Module Identification Register	F000 0308$_H$	0000 C002$_H$
JDP_ID	JTAG/OCDS Module Identification Register	F000 0408$_H$	0000 6305$_H$
IIC_ID	IIC Module Identification Register	F000 0508$_H$	0000 4604$_H$
GPTU0_ID	GPTU Module Identification Register	F000 0708$_H$	0001 C002$_H$
GPTU1_ID	GPTU Module Identification Register	F000 0608$_H$	0001 C002$_H$
SSC_ID	SSC Module Identification Register	F000 0808$_H$	0000 4503$_H$
ASC0_ID	ASC Module Identification Register	F000 0A08$_H$	0000 44E1$_H$
ASC1_ID	ASC Module Identification Register	F000 0B08$_H$	0000 44E1$_H$
ASC2_ID	ASC Module Identification Register	F000 0C08$_H$	0000 44E1$_H$
ADC_ID	ADC Module Identification Register	F000 2208$_H$	0000 3104$_H$
CODEC_ID	Codec Identification Register	F000 2408$_H$	001C C002$_H$
SDLM_ID	SDLM Module Identification Register	F000 2608$_H$	0000 4204$_H$
PCP_ID	PCP Module Identification Register	F000 3F08$_H$	0020 C003$_H$
CAN_ID	CAN Module Identification Register	F010 0008$_H$	0000 4110$_H$
CPS_ID	CPU Module Identification Register	F7E0 FE08$_H$	0015 C004$_H$
MMU_ID	MMU Identification Register	F7E1 8008$_H$	0009 C002$_H$
CPU_ID	CPU Identification Register	F7E1 FE18$_H$	000A C003$_H$
EBU_ID	EBU_LMB Identification Register	F800 0008$_H$	0014 C003$_H$
DMU_ID	DMU Identification Register	F87F FC08$_H$	0008 C002$_H$
PMU_ID	PMU Module Identification Register	F87F FD08$_H$	000B C002$_H$
LCU_ID	LCU Identification Register	F87F FE08$_H$	000F C003$_H$
LFI_ID	LFI Identification Register	F87F FF08$_H$	000C C003$_H$

Preliminary

Electrical characteristics

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the TC1920 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the TC1920 will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the TC1920.

Preliminary

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	85	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	
Junction temperature	T_J	–	125	°C	under bias
Voltage on I/O Supply pins with respect to ground (V_{SS})	V_{DDP}	-0.5	4.2	V	
Voltage on Core Supply pins with respect to ground (V_{SS})	V_{DD}	-0.3	2.1	V	
Voltage on PLL Supply pins with respect to ground (V_{SS})	V_{DDPLL}	-0.3	2.1	V	PLL
Voltage between Oscillator Supply Pins and ground (V_{SS}).	V_{DDOSC}	-0.3	2.1	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	4.2	V	
Input current on any pin during overload condition	I_{OV}	-10	10	mA	
Absolute sum of all input currents at overload condition	ΣI_{OV}	–	|100|	mA	
Power dissipation	P_{DISS}	–	1.4	W	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN}>V_{DD}$ or $V_{IN}<V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Preliminary

Package Parameters (P-LBGA-260)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Power dissipation	P_{DISS}	–	1.4	W	–
Thermal resistance	R_{THA}	–	27.8	K/W	Chip to ambient

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1920. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DDP}	3.0	3.6[1)]	V	I/O supply
	V_{DD}	1.71	1.89[2)]	V	Core supply
	V_{DDPLL}	1.71	1.89	V	PLL supply
	V_{DDOSC}	1.71	1.89	V	Oscillator supply
Ground voltage	V_{SS}	0		V	
Input current on any pin during overload condition	I_{OV}	-5	5	mA	$V_{OV} > V_{DDP}$ + 0.3V $V_{OV} < V_{SS}$ - 0.3V
Absolute sum of all input currents at overload condition	$\Sigma\lvert I_{OV}\rvert$	–	|50|	mA	
Ambient temperature under bias	T_A	-40	85	°C	
CPU clock	f_{CPU}	–	100	MHz	
External Load Capacitance	C_L	–	50	pF	

1) Voltage overshoot to 4 V is permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h

2) Voltage overshoot to 2 V is permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h

Preliminary

DC Characteristics

GPIO pins

Parameter	Symbol	Limit values		Unit	Test Conditions
		min.	max.		
Output low voltage (strong driver)	V_{OL}	-	1 0.4	V	I_{OL} = 10 mA I_{OL} = 2.5 mA
Output high voltage (strong driver)	V_{OH}	2.4	-	V	I_{OH} = - 2.5 mA
Output low voltage (medium driver)[1)]	V_{OL}	-	0.4	V	I_{OL} = 1 mA
Output high voltage (medium driver)[1)]	V_{OH}	2.4	-	V	I_{OH} = - 1 mA
Output low voltage (weak driver)[1)]	V_{OL}	-	0.4	V	I_{OL} = 100 µA
Output high voltage (weak driver)[1)]	V_{OH}	2.4	-	V	I_{OH} = - 100 µA
Input low voltage	V_{IL}	-0.3	0.8	V	LVTTL
Input high voltage	V_{IH}	2.0	V_{DDP}+0.3 or 3.7V	V	whatever is lower
Input leakage current	I_{OZ1}	-	±500	nA	0V< V_{in} < V_{DDP}
Pull-up current [2)]	$\|I_{PUH}\|$	-	1	µA	V_{OUT} = 2.0V
Pull-up current [3)]	$\|I_{PUL}\|$	20	-	µA	V_{OUT} = 0.8V
Pull-down current	$\|I_{PDL}\|$	-	0.8	µA	V_{OUT} = 0.8V
Pull-down current	$\|I_{PDH}\|$	20	-	µA	V_{OUT} = 2.0V
Pin capacitance[1)]	C_{IO}	-	10	pF	f = 1MHz @ T_A = 25°C

1) Not subject to production test, verified by design/characterization.

2) The maximum current that may be drawn while the respective signal line remains inactive.

3) The minimum current that must be drawn in order to drive the respective signal line active.

Preliminary

NMI Pin

NMI Pin is an input pin with different Pull-Up characteristics than other pins. The related characteristics are given in the following table

Parameter	Symbol	Limit values		Unit	Test Conditions
		min.	max.		
Max. current allowed through the Pull-Up device while pin (input) voltage remains still at the high level	$\|I_{PUH}\|$	-	4	uA	V_{OUT}=2.0V
Min. current needed through the Pull-Up device so that pin voltage is driven to the low level.	$\|I_{PUL}\|$	100	-	uA	V_{OUT}=0.8V

Note: NMI Pin does not have a Pull-Down device.

Oscillator Pins

Parameter	Symbol	Limit values		Unit	Test Conditions
		min.	max.		
Input leakage current (analog input) at XTAL1[1)]	I_{OZ1} CC	-	±200	nA	0V< V_{in} < V_{DDP}
Input low voltage XTAL1	V_{ILX} SR	-	0.3	V	-
Input high voltage XTAL1[2)]	V_{IHX} SR	0.8	V_{DD}-0.3 V_{DD}-0.35 V_{DD}-0.4 V_{DD}-0.43	V	f_{OSC}=4MHz f_{OSC}=8MHz f_{OSC}=12MHz f_{OSC}=16MHz
XTAL1 input current	I_{IX1} CC	-	±20	µA	0V < V_{IN} < V_{DD}
XTAL3 input current[2)]	I_{IX3} CC	-	±0.5	µA	0V < V_{IN} < V_{DD}

1) Only applicable in deep sleep mode

2) Not subject to production test, verified by design/characterization.

Preliminary

IIC Pins

Each IIC Pin is an open drain output pin with different characteristics than other pins. The related characteristics are given in the following table

Parameter	Symbol	Limit values		Unit	Test Conditions
		min.	max.		
Output low voltage	V_{OL} CC	-	0.4 0.6	V	3 mA 6 mA
Input high voltage[1)]	V_{IH} SR	$0.7V_{DDP}$	3.6	V	-
Input low voltage[1)]	V_{IL} SR	-0.3	$0.3V_{DDP}$	V	-
Input leakage current	I_{OZ2} CC	-	+ - 500	nA	
Pin capacitance[1)]	C_{IO} CC	-	10	pF	f=1MHz@ T_A=25°C

1) Not subject to production test, verified by design/characterization.

Note: No 5 V IIC interface is supported with these pads. Only voltages lower than 3.60 V must be applied to these pads.

Note: IIC pins have no Pull-Up and Pull-Down devices.

Preliminary

ADC Analog I/O DC Characteristics

Parameter	Symbol	Limit values			Unit	Test Conditions
		min.	typ.	max.		
Core supply voltage	V_{DD} SR	1.71	1.8	1.89	V	-
Analog supply voltage	V_{DDA} SR	3.0	3.3	3.6	V	-
Analog supply ground	V_{SSA} SR	-0.1	0.0	+0.1	V	-
Reference voltage[3)]	V_{AREF}	1.5	-	V_{DDA}+ 0.05	V	-
Reference ground	V_{AGND}	V_{SSA} - 0.05	V_{SSA}	V_{SSA} + 0.05	V	-
Analog input voltage	V_A	V_{AGND}	–	V_{AREF}	V	-
Internal A/D Converter clock	f_{ANA}	0.5	–	3.5	MHz	-
Input leakage current (analog input)	I_{OZ1} CC	-		±200	nA	0V< V_{in} < V_{DDA}
Input leakage current (V_{AGnd} , V_{ARef})	I_{OZ2} CC	-		±500	nA	0V< V_{in} < V_{DDA}
Overload current	I_{AOV} SR	-2		+5	mA	1) 5)
Overload coupling factor[2)]	k_A	-		$1.0x10^{-4}$ $1.5x10^{-3}$	-	I_{AOV}>0 [3)] I_{AOV}<0
Sample time	t_s CC	$4*(CHCON_n.STC+2)*t_{BC}$				for channel n
Conversion time[3)] $t_{BC}=1/f_{BC}$, $t_{DIV}=1/f_{DIV}$, see **Figure 17**.	t_c CC	$t_S + 40*t_{BC} + 2*t_{DIV}$				for 8- bit conversion
		$t_S + 48*t_{BC} + 2*t_{DIV}$				for 10- bit conversion
		$t_S + 56*t_{BC} + 2*t_{DIV}$				for 12- bit conversion

Preliminary

Parameter	Symbol	Limit values			Unit	Test Conditions
		min.	typ.	max.		
Total unadjusted error[4]	TUE CC			±1 LSB		for 8- bit conversion
				±2 LSB		for 10- bit conversion
				±6 LSB[5]		for 12- bit conversion
On resistance of the transmission gates in the analog voltage path[7]	R_{AIN} CC		1900		Ohm	
Resistance of the reference voltage path[7]	R_{REF} CC		2000		Ohm	
Switched capacitance at the analog voltage input.[7]	C_{AINSW} CC		10		pF	
Total capacitance at analog voltage input [6]	C_{AINTOT} CC	-	15	-	pF	
Switched capacitance at the positive reference voltage input.[7]	C_{AREFSW} CC		15		pF	

1) Analog overload conditions during operation occur if the voltage on the respective ADC pin exceeds the specified operating range (i.e. $V_{AOV} > V_{DDP}+0.3V$ *or* $V_{AOV} < V_{SSP}-0.3V$) or a short circuit condition occurs on the respective ADC pin. The absolute sum of input leakage and I_{AOV} currents on all port pins must not exceed **10 mA** at any time. The supply voltage (V_{DD}, V_{DDP} and V_{SS}, V_{SSP}) must remain within the specified limits. Under short-circuit conditions the corresponding pin is not ready for use.

2) The overload coupling factor (k_A) defines the worst case relation of an overload condition (I_{OV}) at one pin to the resulting total leakage current ($I_{leakTOT}$) into an adjacent pin: $|I_{leakTOT}| = k_A \times |I_{OV}| + I_{OZ1V}$
Thus under overload conditions an additional error leakage voltage (V_{AEL}) will be induced onto an adjacent analog input pin due to the resistance of the analog input source (R_{AIN}). That means $V_{AEL} = R_{AIN} \times |I_{leakTOT}|$.
Please see also the analog/digital converter specification, chapter “Error Through Overload Conditions”, for further explanations.

3) The nominal conversion time is valid for V_{AREF}>3.0. For V_{AREF}<3.0, it is approximately double.

4) At V_{AREF}=+3.3V and V_{AGND} in the specified range. For V_{AREF}<3.3V, TUE rise and is to be multiplied with a factor of 3.3/Vref. For V_{AGND} outside the specified range, TUE is not guaranteed.

5) Tested in production on request. Standard production test is 10-bit TUE test.

6) Not subject to production test, verified by design/characterization.

7) Simulation values.

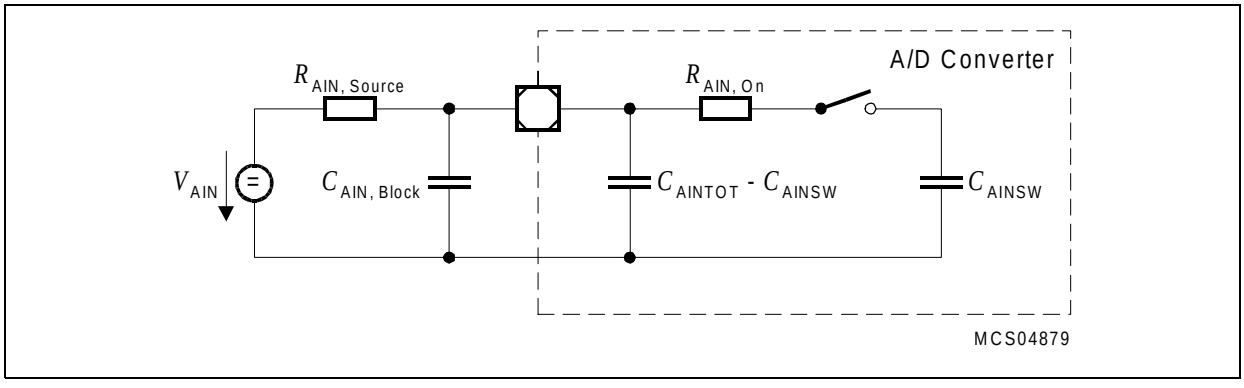


Figure 16 Equivalent Circuitry of an Analog Input

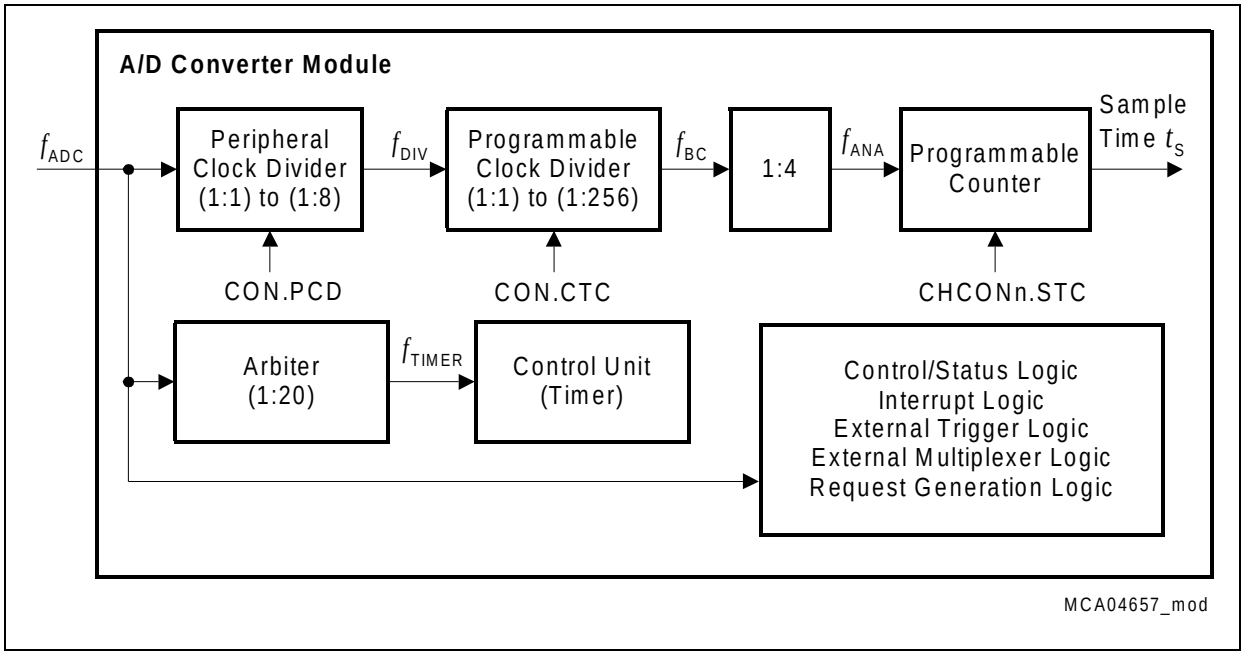


Figure 17 ADC Clock Circuit

Preliminary

Codec Electrical Characteristics

Parameter	Symbol	Limit values			Unit	Test Conditions
		min.	typ.	max.		
Digital supply voltage	V_{DD}	1.71	1.8	1.89	V	
Analog supply voltage	V_{DDA}	3.0	3.3	3.6	V	
Analog supply ground	V_{SSA}	-0.1	0.0	+0.1	V	
External reference voltage	V_{AREF} [1]	1.14	1.2	+1.26 [2]	V	
Analog reference ground	V_{AGND}	V_{SSA}- 0.05	V_{SSA}	V_{SSA}+ 0.05	V	
Analog input voltage (RMS)	V_{AIN}			0.775	V_{rms}	[3]
Analog output voltage (RMS)	V_{AOUT}			0.775	V_{rms}	
Input Resistace of the Analog Inputs [4]	Ra	-	30	-	kOhm	differential input, gain: -12,-6, 0 dB
		-	15	-	kOhm	single-ended input, gain: -12,-6, 0 dB
		-	60	-	kOhm	differential input, gain: 6 to 30 dB
		-	30	-	kOhm	single-ended input, gain: 6 to 30 dB
Internal Reference Voltage Vref (Bandgap Voltage) [5]	V_{BGP}	1.1	1.2	1.3	V	AGCCR. BGPSEL[1,0] =00

1) Reference voltage outside the nominal range causes reduced dynamic range, decreased distortion/clipping margins, increased/decreased gain.

2) $V_{SSA}=V_{AGND}=0V$

3) Please take the gain settings of the analog preamplifier into account, therefore $V_{imaxreal}=V_{imax}$/gain

4) Simulation value.

5) For external usage only, Bandgap reference voltage is strongly dependent on the external load (<500 MOhm). In this case, high impedance buffer must be used.

Preliminary

Codec ADC and DAC path characteristics

Parameters	min.	typ.	max.	Unit	Test conditions[1]
Attenuation distortion (ref. freq. 1014 Hz) (ref. level 0dBm0)[2]	0 -0.25 -0.25 -0.25 0		 0.25 0.45	dB dB dB dB dB	< 0.025 0.025-0.0375 0.0375-0.3 0.3-0.425 > 0.425
Signal to total distor-tion		-55	-45	dB	at 0dBm0
Gain tracking (ref. freq. 1014 Hz) (ref. level 0dBm0)[2]	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
Idle channel noise		-80	-75	dBm 0	receive &transmit
Cross talk		-80	-75	dB	
Harmonic distortion		-60	-50	dB	at 0dBm0
Gain (ref. freq. 1014 Hz) (ref. level 0dBm0)[2]	-0.8	0	0.8	dB	receive &transmit
Power supply rejection ratio (PSRR)	-	-60 -40	-35 -35	dB dB	Receive (0.0375-0.425)[3] Transmit (0.0375-0.425)[3]

1) Values given in this table are valid for all sampling frequencies.

2) 0dBm0 is equivalent to -12dBm is equal to 194.7 mV_{RMS}.

3) Supply ripple 70 mV.

Note: Numbers without units in the test conditions column are relative frequency values to the chosen sampling frequency. e.g. 0.425 equals 3.4 kHz @ 8 kHz sampling frequency.

Preliminary

Power Supply Current

Parameter	Symbol	Limit values		Unit	Test Conditions
		typ. [1]	max.		
Active mode supply current[2] [3]	I_{DD}	260	–	mA	Sum of all I_{DD}.
Idle mode supply current[4]	I_{ID}	170	–	mA	at 1.8V Core Supply
Deep sleep mode supply current	I_{DDS}	0.25	–	mA	at 1.8V Core Supply

1) Typical values are measured at 25°C, CPU clock at 100MHz and nominal supply voltage, i.e. 3.3V for V_{DDP} and 1.8V for V_{DD}, V_{DDPLL}, V_{DDOSC}

2) $\overline{PORST}=V_{IH}$

3) The typical power consumption values in active mode are measured while running a typical application pattern. The power consumption of modules can increase or decrease using different application programs. The PLL is bypassed and powered down during this measurement.

4) CPU is in idle state, input clock to all peripherals are enabled.

AC Characteristics

Operating Conditions apply.

Output Rise/Fall Times

GPIO pins

Rise/fall time measurements are made between 10% and 90%.

The following table is valid for the GPIO pins pad drivers. Output pad characteristics are controllable via DRVCTRx registers.

Pad Modus rise / fall time	Symbol	Limit values		Temp Comp	Unit	Test Conditions
		min.	max.			
Strong driver						
• sharp edge	SF	-	3	yes	ns	@50pF
• medium edge[1]	SM	-	6	yes	ns	@50pF
• soft edge[1]	SS	-	12	yes	ns	@50pF

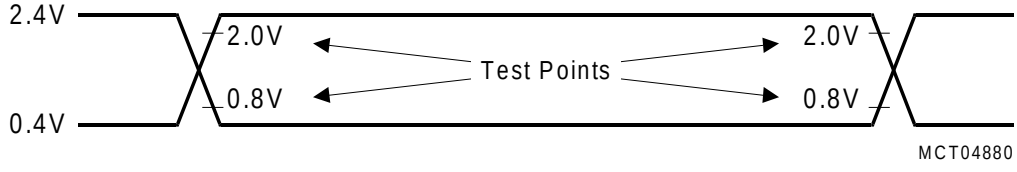
1) Not subject to production test, verified by design/characterization.

Preliminary

Timing Characteristics

(Operating Conditions apply)

Note: Timing parameters are not subject to production test, they are verified by design/ characterization.



AC inputs during testing are driven at 2.4V for a logic “1” and 0.4V for a logic “0”. Timing measurements are made at V_{IHmin} for a logic “1” and V_{ILmax} for a logic “0”.

Figure 18 Input/Output Waveforms for AC Tests - for GPIO, Dedicated and EBU pins

External Oscillator at XTAL1 Timing Requirements

(Operating Conditions apply)

Parameter		Symbol		Limits		Unit
				min.	max.	
Main Oscillator XTAL frequency[1]	with/without PLL	f_{OSC}	SR	4	16	MHz
Frequency of an external oscillator driving at XTAL1[2]	with PLL[3] without PLL[4]	f_{OSCDD}	SR SR	4 -	25 25	MHz
Input Clock high time		t_1	SR	16	–	ns
Input Clock low time		t_2	SR	16	–	ns
Input Clock rise time		t_3	SR	–	7	ns
Input Clock fall time		t_4	SR	–	7	ns

1) Oscillator Bypass Pin P3.11 latch-in value high. Internal oscillator provides the input clock signal.

2) Oscillator Bypass Pin P3.11 latch-in value low. Internal oscillator disabled. External oscillator provides the input clock signal.

3) Internal PLL provides the system clock. BYPASS pin latch-in value low. PLL prescaler value P=1.

4) Internal PLL bypassed. BYPASS pin latch-in value high. External oscillator provides the system clock directly. When ADC and CODEC modules are active their frequency limitations must be taken into consideration, together with LMB/FPI bus frequency ratio. Otherwise, minimum frequency in this mode can go as low as zero.

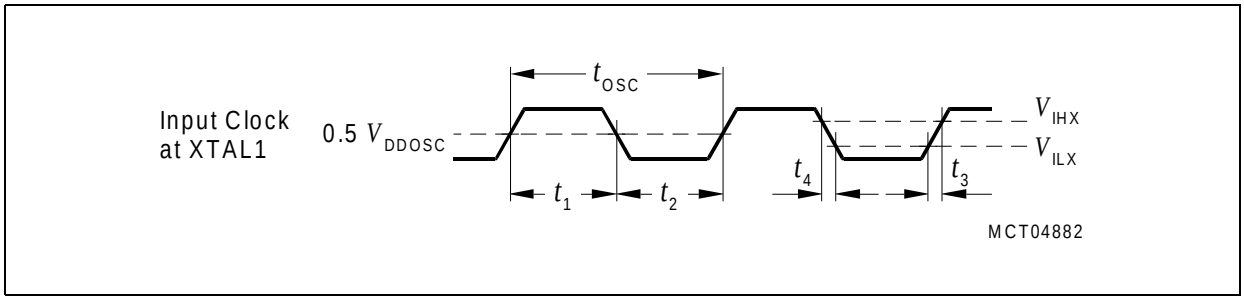


Figure 19 External Clock at XTAL1 Requirements

Note: V_{DDOSC}, V_{IHX} and V_{IHL} are defined in the Oscillator Pins DC Characteristics Chapter.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

Preliminary

CPU Clock Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min.	max.	
CLKOUT period	t_{CLKOUT} CC	10	–	ns
CLKOUT high time	t_1 CC	4	–	ns
CLKOUT low time	t_2 CC	4	–	ns
CLKOUT rise time	t_3 CC	–	3	ns
CLKOUT fall time	t_4 CC	–	3	ns

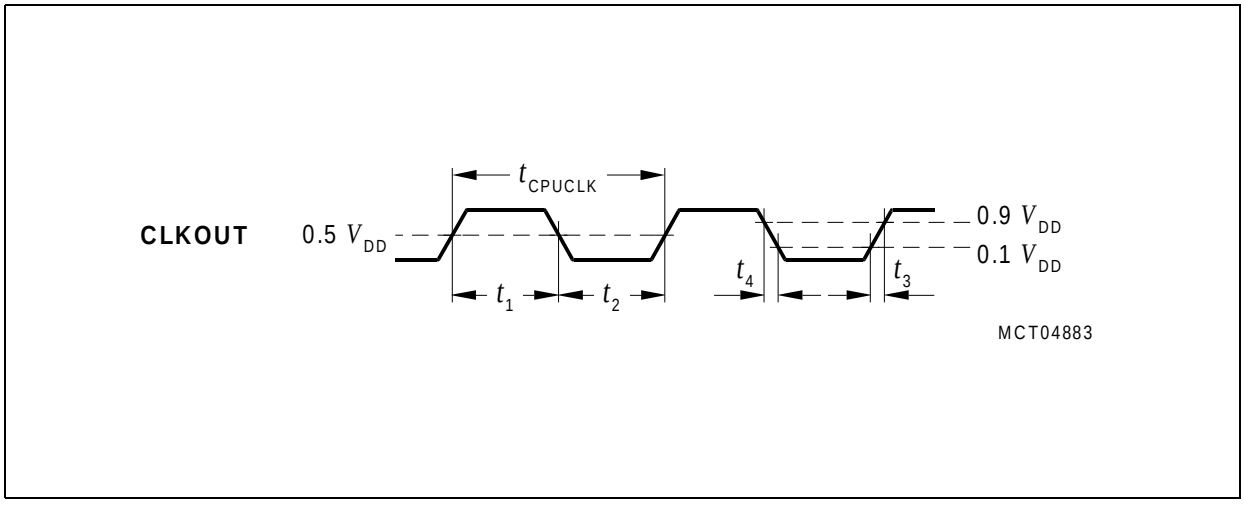


Figure 20 CLKOUT Timing

Preliminary

PLL Parameters

Parameter	Symbol	Limit Values[1]		Unit
		min.	max.	
Accumulated jitter	D_N	see Figure 21		–
VCO frequency range	f_{VCO}	100	150[2]	MHz
		150	200[3]	MHz
		200	250[4]	MHz
		250	300[5]	MHz
PLL base frequency	$f_{PLLBASE}$	20	80[2]	MHz
		20	130[3]	MHz
		20	180[4]	MHz
		20	230[5]	MHz
PLL lock-in time	t_L	–	200	µs

1) Not subject to production test, verified by design/characterization.

2) @ vcosel = ’00’

3) @ vcosel = ’01’

4) @ vcosel = ’10’

5) @ vcosel = ’11’

Note: When TC1920 starts-up with the PLL not bypassed, first user instructions are executed with the frequency defined by the VCO free-running frequency ($f_{PLLBASE}$) and by the reset value of the PLL_CLC register (the K-divider and VCOSEL bitfields). It is software responsibility to initialize its own appropriate values in the bitfields in this register, before giving the command for the VCO to lock to the input frequency. For more information, see the Users Manual, System Units, System Control Unit chapter.

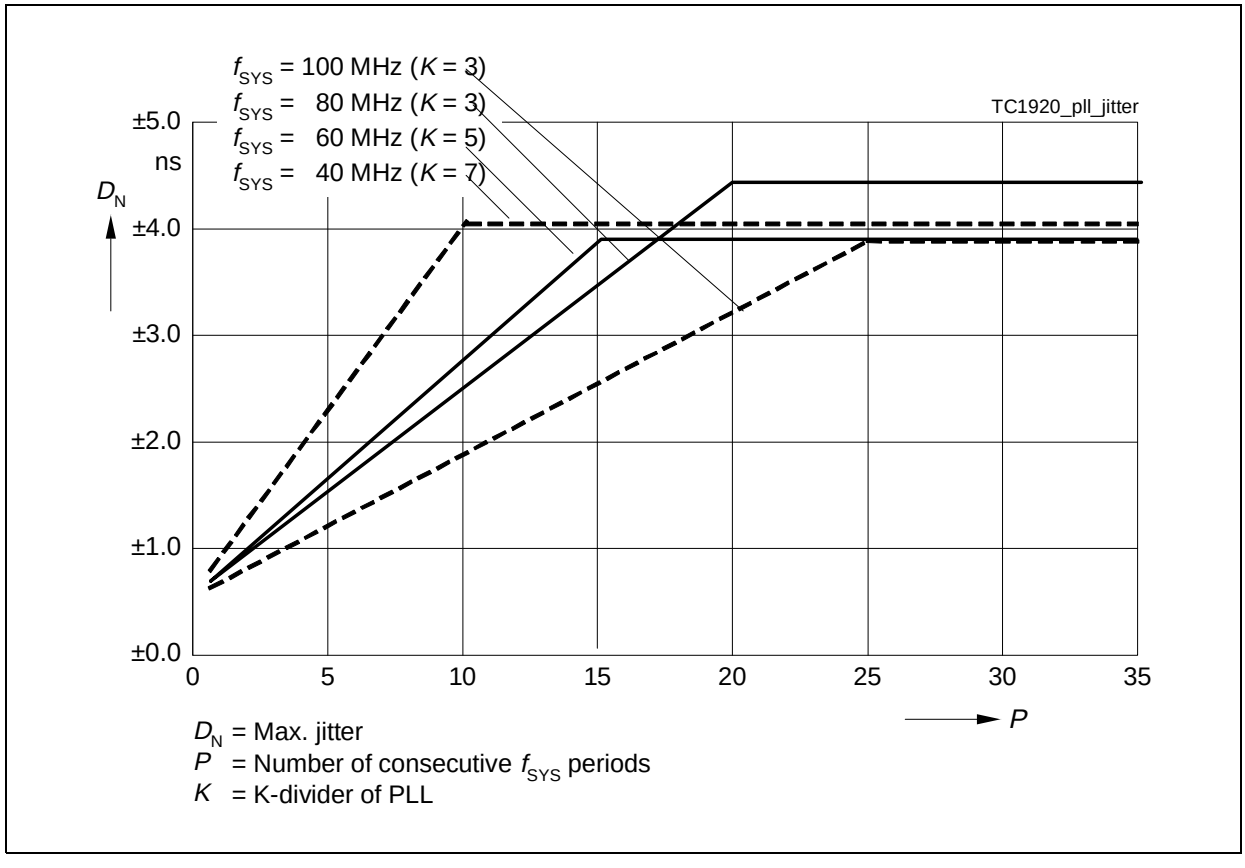


Figure 21 Approximated Maximum Accumulated PLL Jitter

The following two formulas define the (absolute) approximate maximum value of jitter D_N in [ns] dependent on the K-factor, the system clock frequency f_{SYS} in [MHz], and the number P of consecutive f_{SYS} periods.

$$\text{for } P < 0.25 \times f_{SYS} \quad D_N\,[\text{ns}] = \pm\left[\left(\frac{735}{f_{SYS} \times K} + 0.9\right) \times \frac{P}{f_{SYS} \times 0.25} + 0.5\right] \quad [1]$$

$$\text{for } P \geq 0.25 \times f_{SYS} \quad D_N\,[\text{ns}] = \pm\left[\frac{735}{f_{SYS} \times K} + 1.4\right] \quad [2]$$

With rising number P of clock cycles the maximum jitter increases linearly up to a specific value of P. Beyond this value of P the maximum accumulated jitter remains at a constant value.

Preliminary

Timing for EBU_LMB Clock Outputs

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
EBUCLK period	t_1	CC	10	–	ns
EBUCLK high time	t_2	CC	4.5	–	ns
EBUCLK low time	t_3	CC	3	–	ns
EBUCLK rise time	t_4	CC	–	2.5	ns
EBUCLK fall time	t_5	CC	–	2.5	ns
BFCLK0 period	t_6	CC	20	–	ns
BFCLK0 high time	t_7	CC	9	–	ns
BFCLK0 low time	t_8	CC	9	–	ns
BFCLK0 rise time	t_9	CC	–	3.5	ns
BFCLK0 fall time	t_{10}	CC	–	2.5	ns

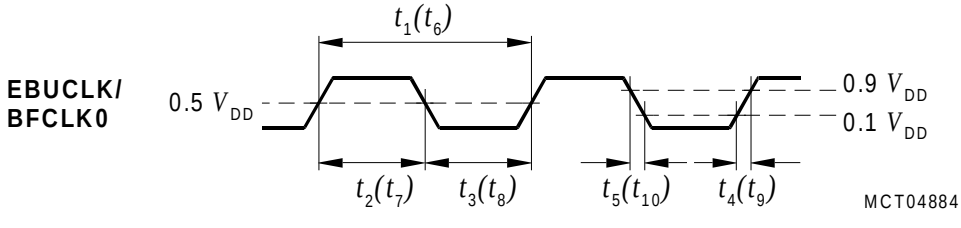


Figure 22 EBU_LMB Clock Output Timing

Preliminary

Timing for SDRAM Access Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
CKE high from EBUCLK ↑	t_1	CC	-	7.0	ns
CKE low from EBUCLK ↑	t_2	CC	2.0	-	ns
A(23:0) output valid from EBUCLK ↑	t_3	CC	-	7.0	ns
A(23:0) output hold from EBUCLK ↑	t_4	CC	2.0	-	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↑	t_5	CC	-	7.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↑	t_6	CC	2.0	-	ns
$\overline{\text{RAS}}$ low from EBUCLK ↑	t_7	CC	-	7.0	ns
$\overline{\text{RAS}}$ high from EBUCLK ↑	t_8	CC	2.0	-	ns
$\overline{\text{CAS}}$ low from EBUCLK ↑	t_9	CC	-	7.0	ns
$\overline{\text{CAS}}$ high from EBUCLK ↑	t_{10}	CC	2.0	-	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↑	t_{11}	CC	-	7.0	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↑	t_{12}	CC	2.0	-	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↑	t_{13}	CC	-	7.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↑	t_{14}	CC	2.0	-	ns
AD(31:0) output valid from EBUCLK ↑	t_{15}	CC	-	7.7	ns
AD(31:0) output hold from EBUCLK ↑	t_{16}	CC	2.0	-	ns
AD(31:0) input setup to EBUCLK ↑	t_{17}	SR	2.0	-	ns
AD(31:0) input hold from EBUCLK ↑	t_{18}	SR	4.0	-	ns

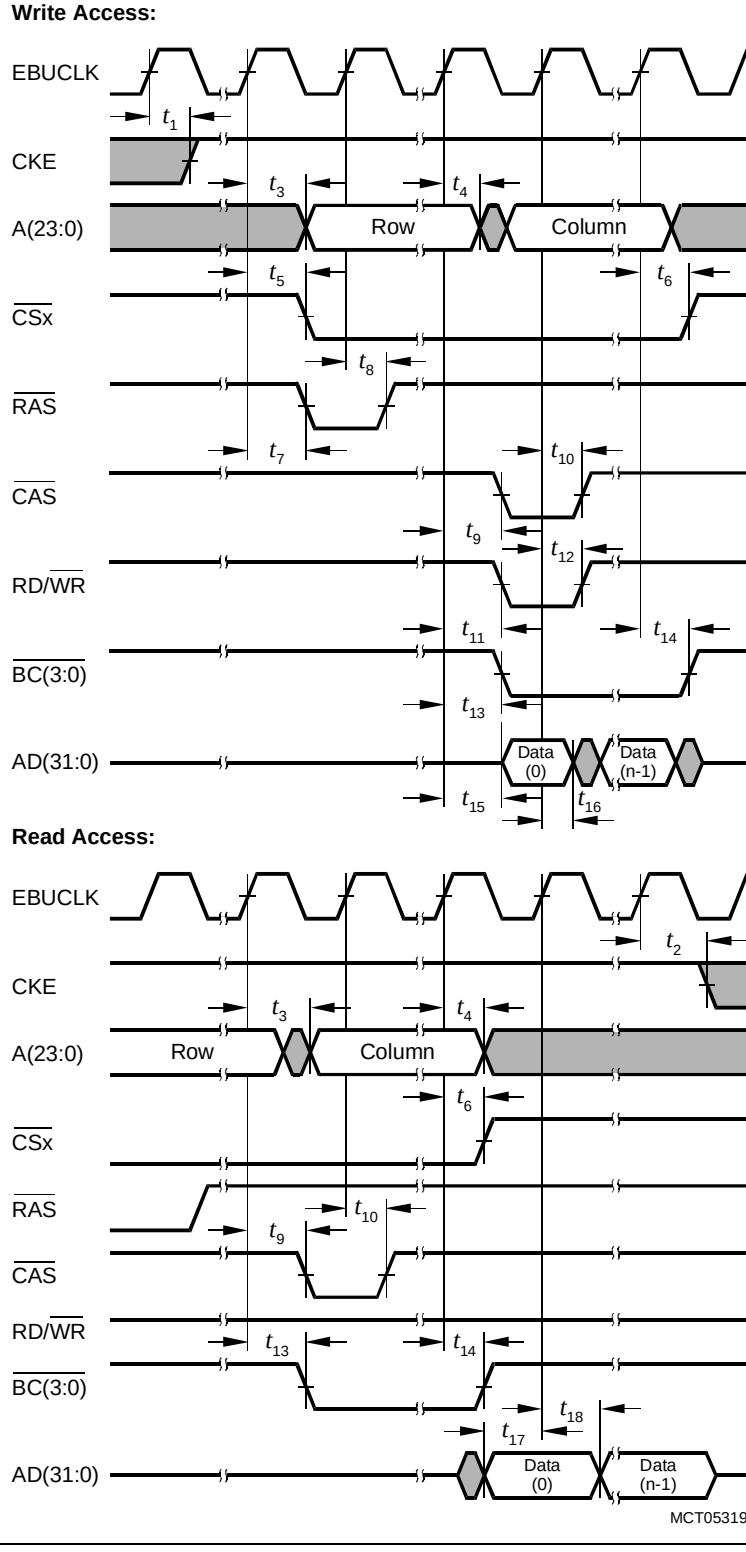


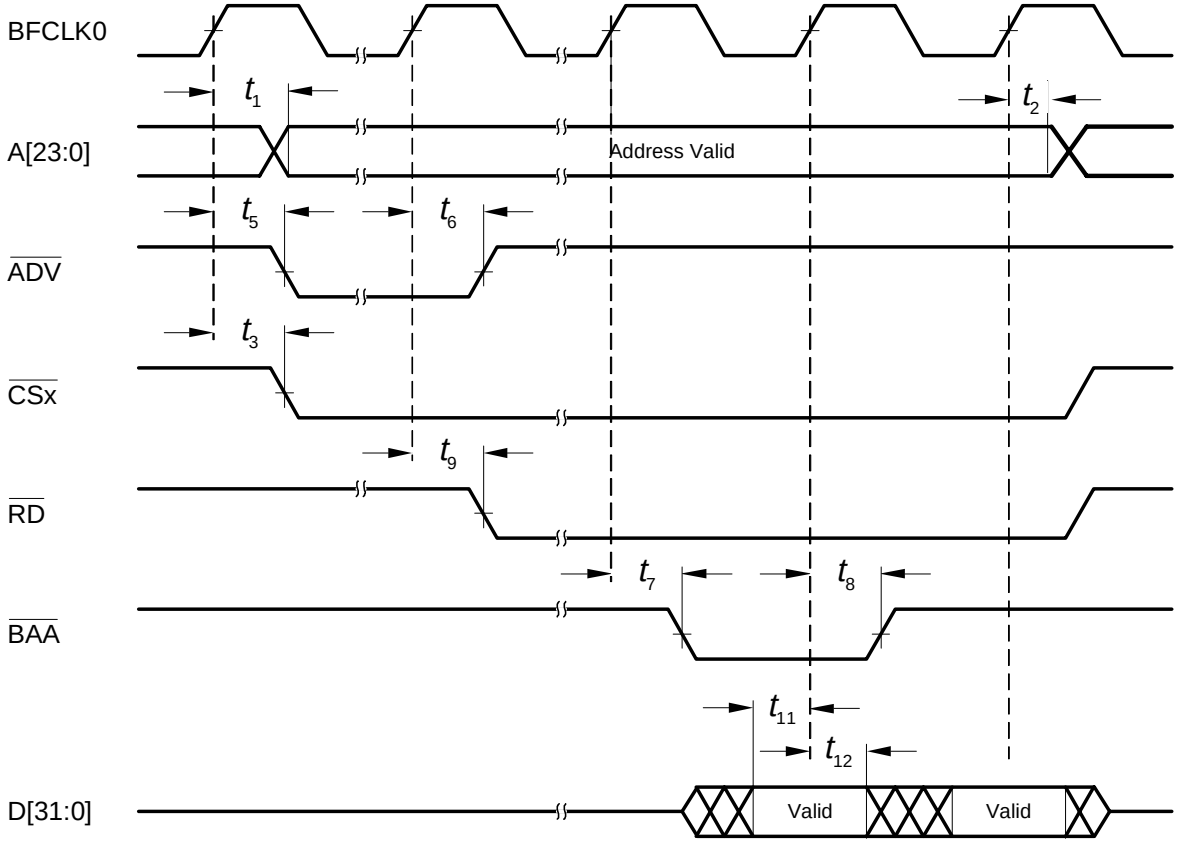
Figure 23 SDRAM Access Timing

Preliminary

Timing for Burst Flash Access Signals

Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
A(23:0) output valid from BFCLK0 ↓	t_1	CC	–	11.0	ns
A(23:0) output hold from BFCLK0 ↓	t_2	CC	0.0	–	ns
$\overline{\text{CS}}$(6:0) low from BFCLK0 ↓	t_3	CC	–	9.0	ns
$\overline{\text{ADV}}$ low from BFCLK0 ↓	t_5	CC	–	10.0	ns
$\overline{\text{ADV}}$ high from BFCLK0 ↓	t_6	CC	3.0	–	ns
$\overline{\text{BAA}}$ low from BFCLK0 ↓	t_7	CC	–	10.0	ns
$\overline{\text{BAA}}$ high from BFCLK0 ↓	t_8	CC	3.0	–	ns
$\overline{\text{RD}}$ low from BFCLK0 ↓	t_9	CC	–	10.0	ns
AD(31:0) input setup to BFCLK0 ↓	t_{11}	SR	6.0	–	ns
AD(31:0) input hold from BFCLK0 ↓	t_{12}	SR	3.0	–	ns



Note: Between the end of the Address Phase ($\overline{ADV}$ goes high) and the beginning of the Command Phase ($\overline{RD}$ goes low) several cycles of Command Delay Phase can be inserted.

mct04889_mod_la

Figure 24 Burst Flash Access Timing (Instruction Read)

Preliminary

Timing for Demultiplexed Access Signals[1)]

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
ALE high from EBUCLK ↑	t_1	CC	–	8.0	ns
ALE low from EBUCLK ↑	t_2	CC	2.0	–	ns
A(23:0) output valid from EBUCLK ↑	t_3	CC	–	8.0	ns
A(23:0) output hold from EBUCLK ↑	t_4	CC	2.0	–	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↑	t_5	CC	–	8.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↑	t_6	CC	2.0	–	ns
MR/$\overline{\text{W}}$ low from EBUCLK ↑	t_7	CC	–	8.0	ns
MR/$\overline{\text{W}}$ high from EBUCLK ↑	t_8	CC	2.0	–	ns
$\overline{\text{RMW}}$ low from EBUCLK ↑	t_9	CC	–	8.0	ns
$\overline{\text{RMW}}$ high from EBUCLK ↑	t_{10}	CC	1.0	–	ns
$\overline{\text{RD}}$ low from EBUCLK ↑	t_{11}	CC	–	8.0	ns
$\overline{\text{RD}}$ high from EBUCLK ↑	t_{12}	CC	0.0	–	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↑	t_{13}	CC	–	8.0	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↑	t_{14}	CC	2.0		ns
$\overline{\text{CMDELAY}}$ input setup to EBUCLK ↑	t_{15}	SR	4.0	–	ns
$\overline{\text{CMDELAY}}$ hold from EBUCLK ↑	t_{16}	SR	3.0	–	ns
$\overline{\text{WAIT}}$ input setup to EBUCLK ↑	t_{17}	SR	4.0	–	ns
$\overline{\text{WAIT}}$ hold from EBUCLK ↑	t_{18}	SR	3.0	–	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↑	t_{19}	CC	–	8.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↑	t_{20}	CC	2.0	–	ns
AD(31:0) output valid from EBUCLK ↑	t_{21}	CC	–	8.0	ns
AD(31:0) output hold from EBUCLK ↑	t_{22}	CC	0.0	–	ns
AD(31:0) input setup to EBUCLK ↑	t_{23}	SR	4.0	–	ns
AD(31:0) input hold from EBUCLK ↑	t_{24}	SR	4.0	–	ns

1) It is user responsibility to program an appropriate whole number of clock cycles to generate the correct phase length according to the particular asynchronous memory/peripheral device specification.

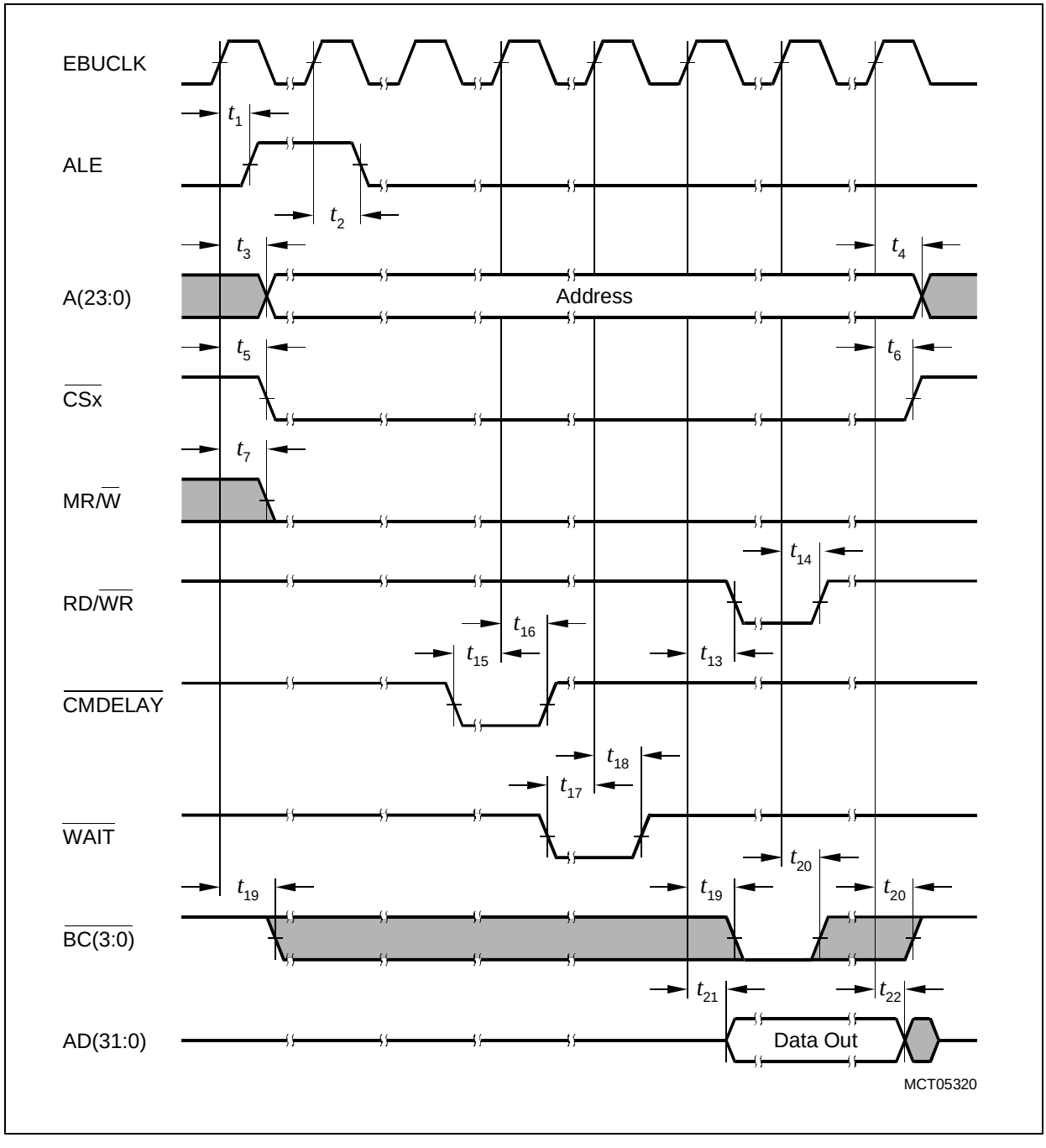


Figure 25 Demultiplexed Write Access

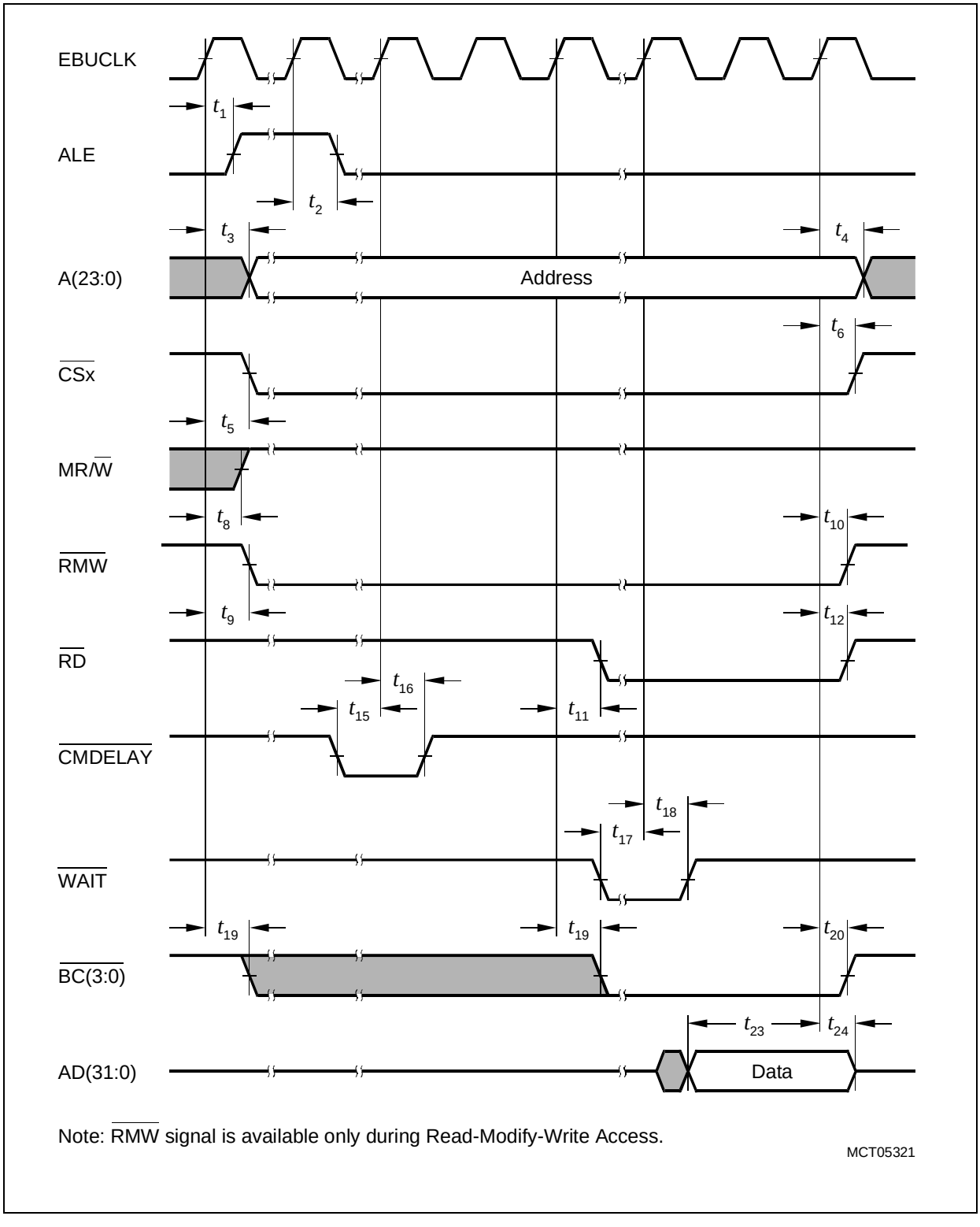


Figure 26 Demultiplexed Read Access

Preliminary

Timing for Multiplexed Access Signals[1)]

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
ALE high from EBUCLK ↑	t_1	CC	–	8.0	ns
ALE low from EBUCLK ↑	t_2	CC	2.0	–	ns
AD(31:0) output valid from EBUCLK ↑	t_3	CC	–	8.0	ns
AD(31:0) output hold from EBUCLK ↑	t_4	CC	0.0	–	ns
AD(31:0) input setup to EBUCLK ↑	t_5	SR	4.0	–	ns
AD(31:0) input hold from EBUCLK ↑	t_6	SR	4.0	–	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↑	t_7	CC	–	8.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↑	t_8	CC	1.0	–	ns
MR/$\overline{\text{W}}$ low from EBUCLK ↑	t_9	CC	–	8.0	ns
MR/$\overline{\text{W}}$ high from EBUCLK ↑	t_{10}	CC	2.0	–	ns
$\overline{\text{RMW}}$ low from EBUCLK ↑	t_{11}	CC	–	8.0	ns
$\overline{\text{RMW}}$ high from EBUCLK ↑	t_{12}	CC	1.0	–	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↑	t_{13}	CC	–	8.0	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↑	t_{14}	CC	2.0	–	ns
$\overline{\text{RD}}$ low from EBUCLK ↑	t_{15}	CC	–	8.0	ns
$\overline{\text{RD}}$ high from EBUCLK ↑	t_{16}	CC	0.0	–	ns
$\overline{\text{CMDELAY}}$ input setup to EBUCLK ↑	t_{17}	SR	4.0	–	ns
$\overline{\text{CMDELAY}}$ hold from EBUCLK ↑	t_{18}	SR	3.0	–	ns
$\overline{\text{WAIT}}$ input setup to EBUCLK ↑	t_{19}	SR	4.0	–	ns
$\overline{\text{WAIT}}$ hold from EBUCLK ↑	t_{20}	SR	3.0	–	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↑	t_{21}	CC	–	8.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↑	t_{22}	CC	2.0	–	ns

1) It is user responsibility to program an appropriate whole number of clock cycles to generate the correct phase length according to the particular asynchronous memory/peripheral device specification.

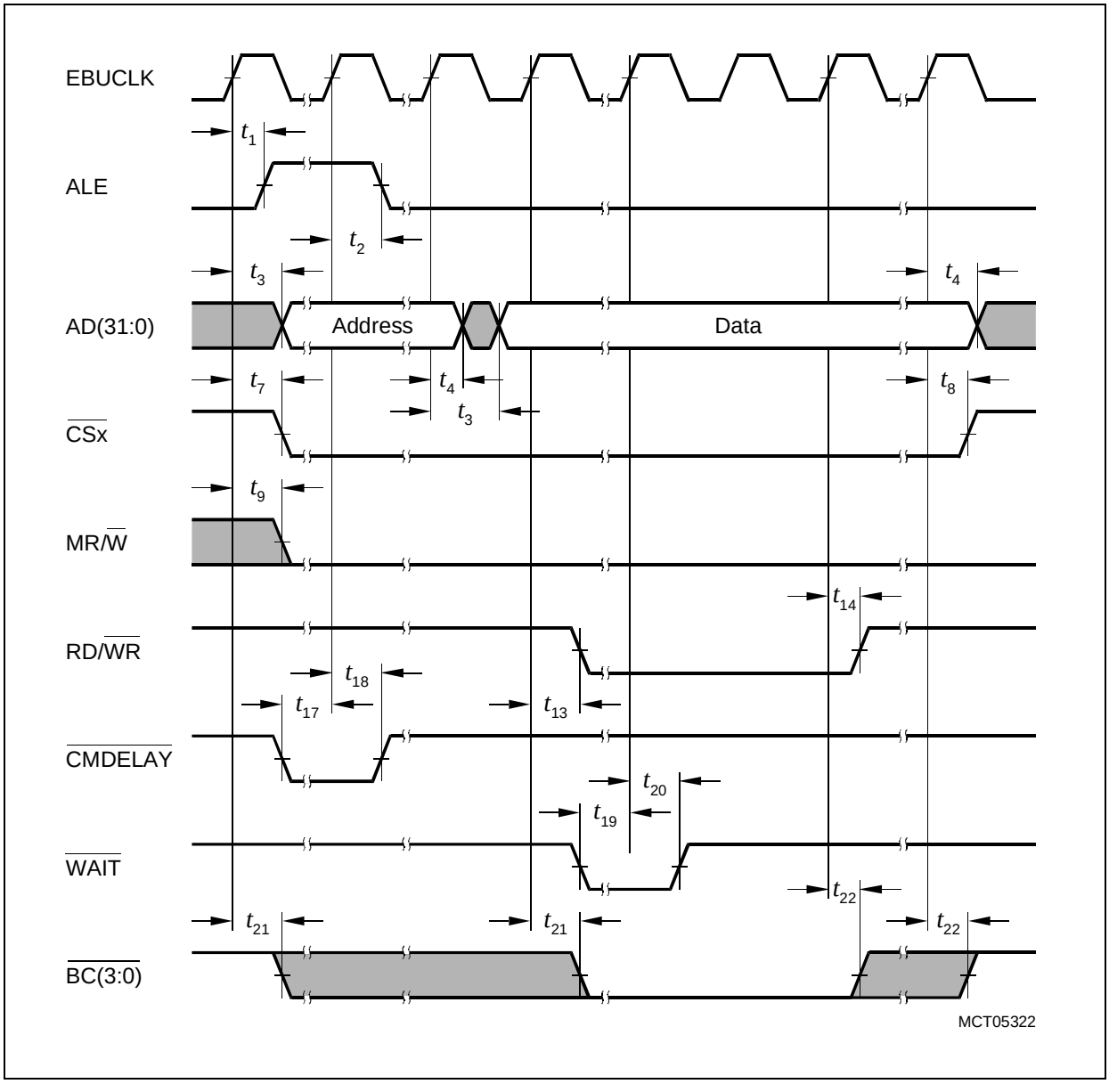


Figure 27 Multiplexed Write Access

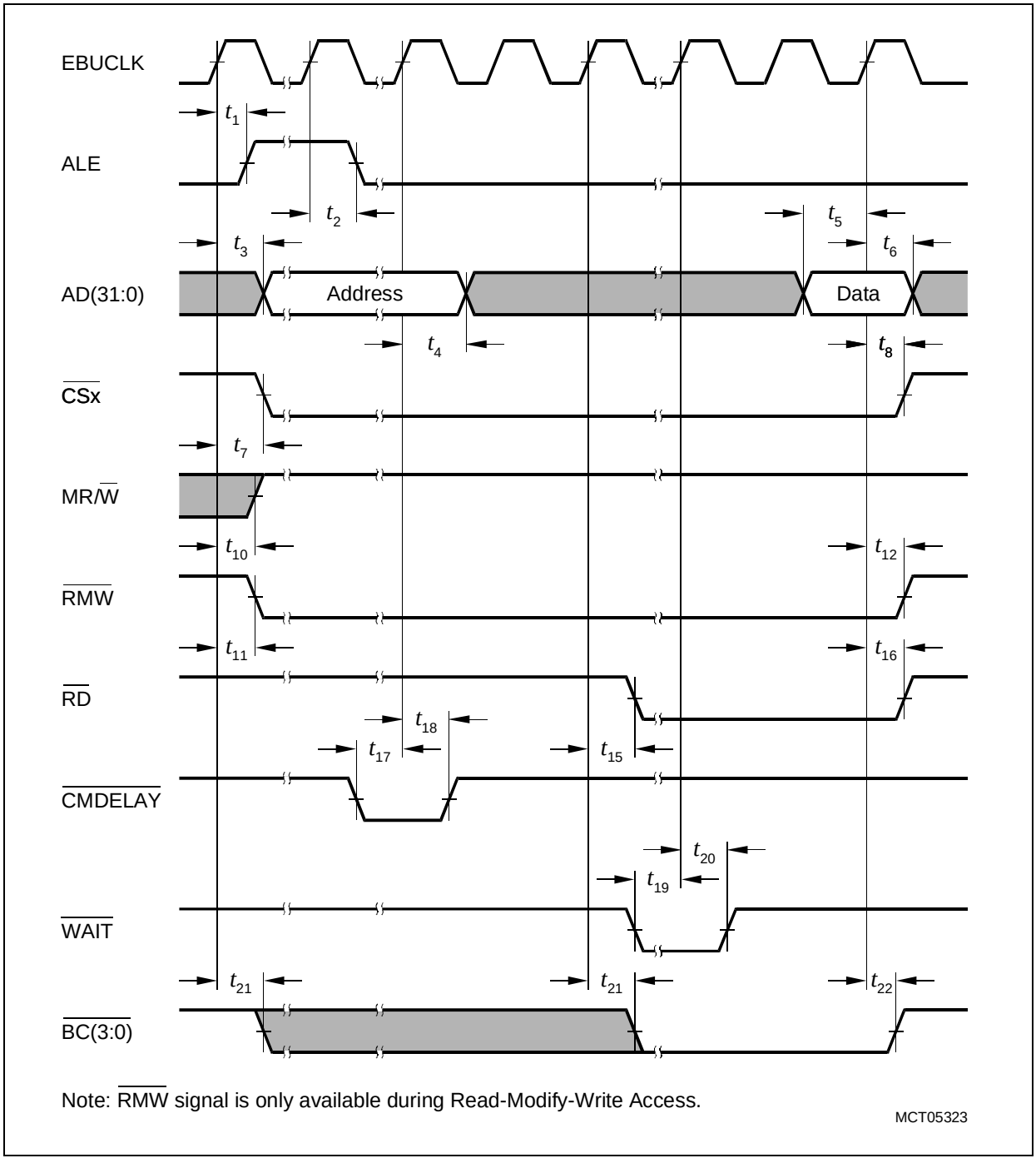


Figure 28 Multiplexed Read Access

Preliminary

Timing for External Bus Arbitration Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
$\overline{\text{HOLD}}$ input setup to EBUCLK ↓	t_1	SR	6.0	–	ns
$\overline{\text{HOLD}}$ input hold from EBUCLK ↓	t_2	SR	8.0	–	ns
$\overline{\text{HLDA}}$ low from EBUCLK ↓	t_3	CC	–	10.0	ns
$\overline{\text{HLDA}}$ high from EBUCLK ↓	t_4	CC	–	9.0	ns
$\overline{\text{HLDA}}$ input setup to EBUCLK ↓	t_5	SR	8.0	–	ns
$\overline{\text{HLDA}}$ input hold from EBUCLK ↓	t_6	SR	8.0	–	ns
$\overline{\text{BREQ}}$ low from EBUCLK ↓	t_7	CC	–	10.0	ns
$\overline{\text{BREQ}}$ high from EBUCLK ↓	t_8	CC	–	9.0	ns

Note: The signals $\overline{HOLD}$, $\overline{HLDA}$ and $\overline{BREQ}$ are alternate function of the $\overline{CS5}$, $\overline{CS6}$ and $\overline{CSOVL}$ Pins.

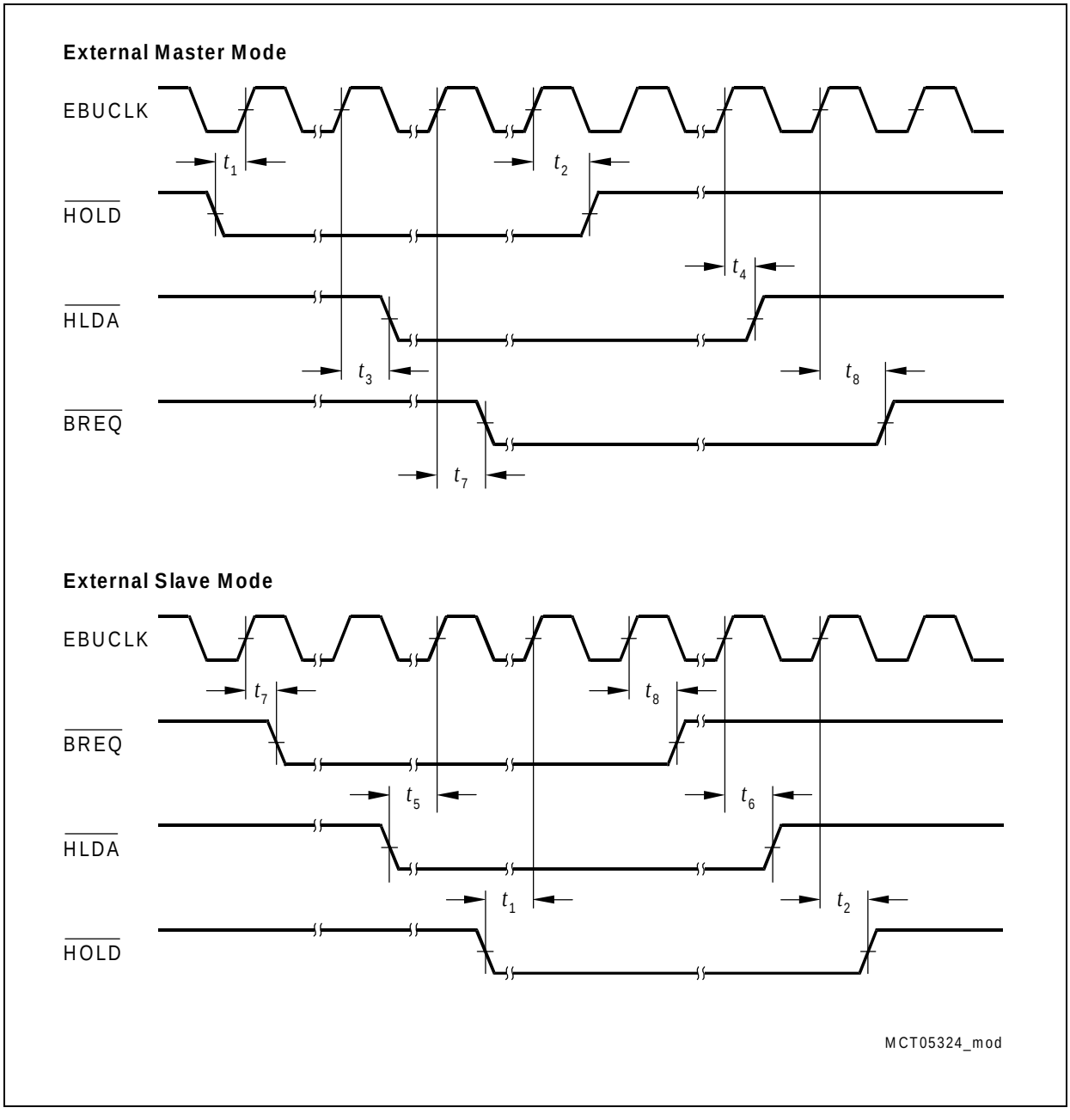


Figure 29 External Bus Arbitration Timing

Preliminary

SSC Master Mode Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK period	t_{SCLK}	CC	40		ns
MTSR low/high from SCLK edge	t_5	CC	-	2.0	ns
MRST setup to SCLK edge	t_6	SR	15	-	ns
MRST hold from SCLK edge	t_7	SR	15	-	ns

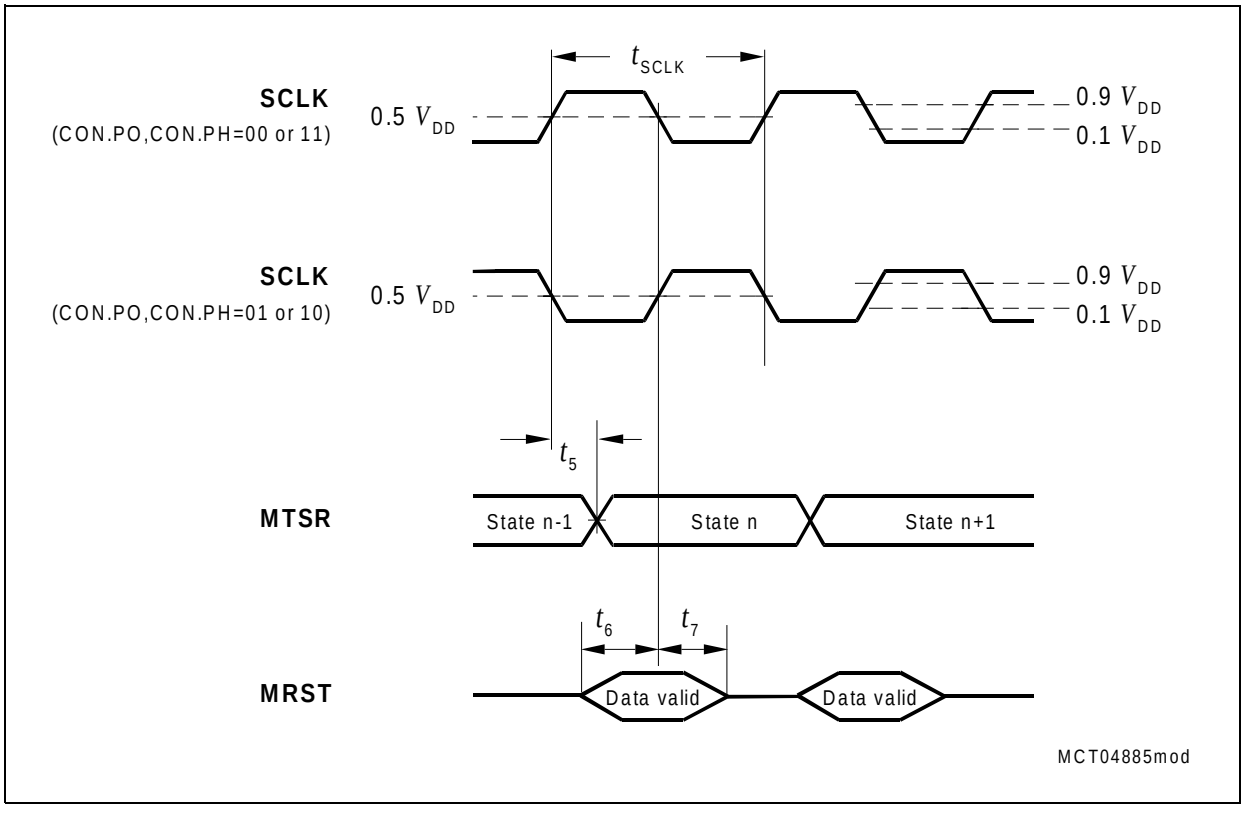


Figure 30 SSC Master Mode Timing

Preliminary

Package Outlines

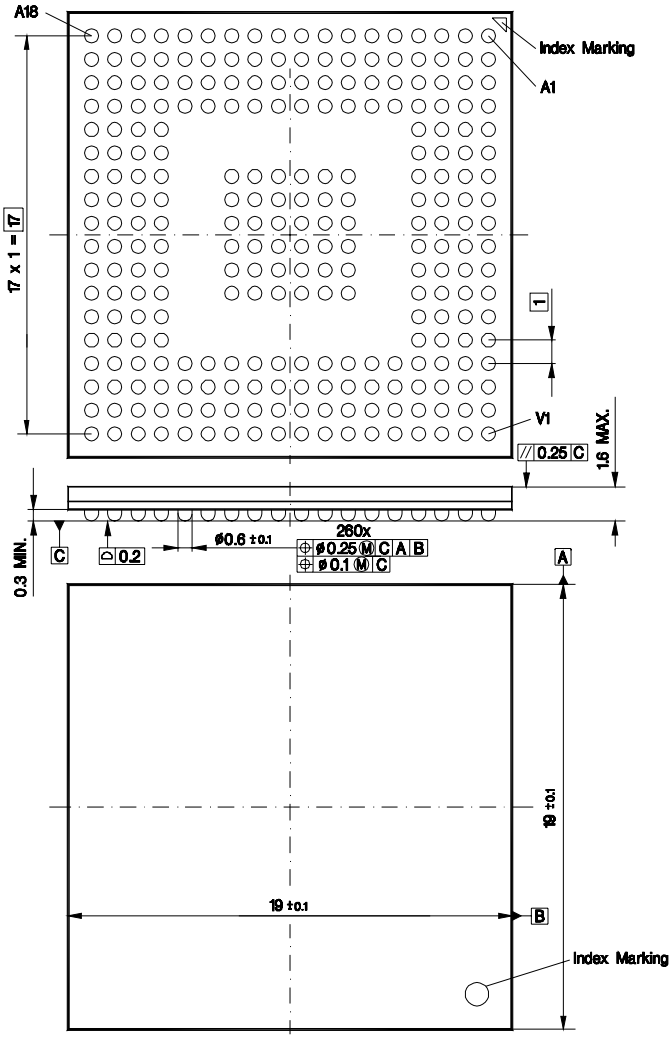


Figure 31 LBGA-260 Package

You can find all of our packages, sorts of packing and other in our Infineon Internet Page “Products”: http://www.infineon.com/products

•

Preliminary

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

http://www.infineon.com

Published by Infineon Technologies AG